

## 650V SuperGaN® FET in TO-247 (source tab)

### Description

The TP65H015G5WS 650V, 15 mΩ gallium nitride GaN FET is a normally-off device using Transphorm's Gen V platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen V SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

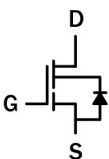
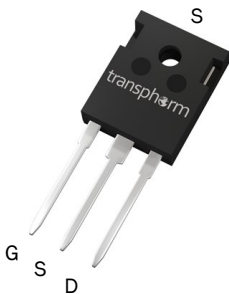
### Related Literature

- [AN0009](#): Recommended External Circuitry for GaN FETs
- [AN0003](#): Printed Circuit Board Layout and Probing
- [AN0010](#): Paralleling GaN FETs

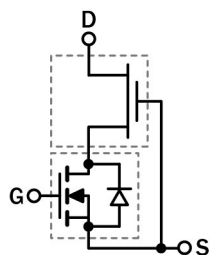
### Ordering Information

Part Number	Package	Package Configuration
TP65H015G5WS	3 lead TO-247	Source

TP65H015G5WS  
TO-247  
(top view)



Cascode Schematic Symbol



Cascode Device Structure

### Features

- JEDEC qualified GaN technology
- Dynamic  $R_{DS(on)eff}$  production tested
- Robust design, defined by
  - Intrinsic lifetime tests
  - Wide gate safety margin
  - Transient over-voltage capability
- Very low  $Q_{RR}$
- Reduced crossover loss

### Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

### Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor



### Key Specifications

$V_{DSS}$ (V)	650
$V_{(TR)DSS}$ (V)	725
$R_{DS(on)eff}$ (mΩ) max*	18
$Q_{RR}$ (nC) typ	430
$Q_G$ (nC) typ	74

\* Dynamic on-resistance; see Figures 18 and 19

# TP65H015G5WS

## Absolute Maximum Ratings ( $T_c=25^\circ\text{C}$ unless otherwise stated.)

Symbol	Parameter		Limit Value	Unit
$V_{DSS}$	Drain to source voltage ( $T_J = -55^\circ\text{C}$ to $150^\circ\text{C}$ )		650	V
$V_{(TR)DSS}$	Transient drain to source voltage <sup>a</sup>		725	
$V_{GSS}$	Gate to source voltage		$\pm 20$	
$P_D$	Maximum power dissipation @ $T_c=25^\circ\text{C}$		266	W
$I_D$	Continuous drain current @ $T_c=25^\circ\text{C}$ <sup>b</sup>		99	A
	Continuous drain current @ $T_c=100^\circ\text{C}$ <sup>b</sup>		62	A
$I_{DM}$	Pulsed drain current (pulse width: 10 $\mu\text{s}$ )		600	A
$T_c$	Operating temperature	Case	-55 to +150	$^\circ\text{C}$
$T_J$		Junction	-55 to +150	$^\circ\text{C}$
$T_S$	Storage temperature		-55 to +150	$^\circ\text{C}$
$T_{SOLD}$	Soldering peak temperature <sup>c</sup>		260	$^\circ\text{C}$

Notes:

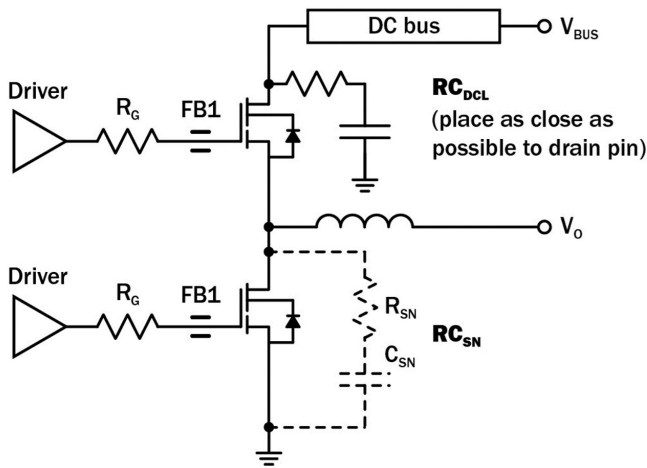
- a. In off-state, spike duty cycle  $D < 0.01$ , spike duration  $< 1\mu\text{s}$
- b. For increased stability at high current operation, see Circuit Implementation on page 3
- c. For 10 sec., 1.6mm from the case

## Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Junction-to-case	0.47	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient	40	$^\circ\text{C/W}$

# TP65H015G5WS

## Circuit Implementation



**Simplified Half-bridge Schematic ( See also on Figure 14 )**

For additional gate driver options/configurations, please see Application Note [AN0009](#)

### Layout Recommendations

#### Gate Loop:

- Gate Driver: SiLab Si823x/Si827x
- Keep gate loop compact
- Minimize coupling with power loop

#### Power loop: ( For reference see page 13 )

- Minimize power loop path inductance
- Minimize switching node coupling with high and low power plane
- Add DC bus snubber to reduce to voltage ringing
- Add Switching node snubber for high current operation

Recommended gate drive: (0V, 12V) with  $R_G=15\Omega$

Gate Ferrite Bead (FB1)	Required DC Link RC Snubber ( $RC_{DCL}$ ) <sup>a</sup>	Recommended Switching Node RC Snubber ( $RC_{SN}$ ) <sup>b,c</sup>
80-120 $\Omega$ at 100MHz	$[10nF + 3.3 \Omega] \times 3$	Not necessary

Notes:

- $RC_{DCL}$  should be placed as close as possible to the drain pin
- $RC_{SN}$  is needed only if  $R_G$  is smaller than recommendations or operational current exceeds 100C rated  $I_{D_{MAX}}$
- If required, please use (100 pF + 10 ohm) or parallel two or three of the same

# TP65H015G5WS

## Electrical Parameters (T<sub>J</sub>=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
<b>Forward Device Characteristics</b>						
V <sub>(BL)DSS</sub>	Drain-source voltage	650	—	—	V	V <sub>GS</sub> =0V
V <sub>GS(th)</sub>	Gate threshold voltage	3.3	4	4.8	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =2mA
R <sub>DS(on)eff</sub>	Drain-source on-resistance <sup>a</sup>	—	15	18	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =60A
		—	27	—		V <sub>GS</sub> =10V, I <sub>D</sub> =60A, T <sub>J</sub> =150 °C
I <sub>DSS</sub>	Drain-to-source leakage current	—	7	70	μA	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V
		—	50	—		V <sub>DS</sub> =650V, V <sub>GS</sub> =0V, T <sub>J</sub> =150 °C
I <sub>GSS</sub>	Gate-to-source forward leakage current	—	—	400	nA	V <sub>GS</sub> =20V
	Gate-to-source reverse leakage current	—	—	-400		V <sub>GS</sub> =-20V
C <sub>ISS</sub>	Input capacitance	—	5218	—	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =400V, f=1MHz
C <sub>OSS</sub>	Output capacitance	—	307	—		
C <sub>RSS</sub>	Reverse transfer capacitance	—	4.5	—		
C <sub>O(er)</sub>	Output capacitance, energy related <sup>b</sup>	—	476	—	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V to 400V
C <sub>O(tr)</sub>	Output capacitance, time related <sup>c</sup>	—	1026	—		
Q <sub>G</sub>	Total gate charge	—	74	100	nC	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V to 10V, I <sub>D</sub> =60A
Q <sub>GS</sub>	Gate-source charge	—	34	—		
Q <sub>GD</sub>	Gate-drain charge	—	21	—		
Q <sub>OSS</sub>	Output charge	—	430	—	nC	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V to 400V
t <sub>D(on)</sub>	Turn-on delay	—	87	—	ns	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V to 12V, R <sub>G</sub> =15Ω, Z <sub>FB</sub> =120Ω at 100MHz, I <sub>D</sub> =60A
t <sub>R</sub>	Rise time	—	18	—		
t <sub>D(off)</sub>	Turn-off delay	—	123	—		
t <sub>F</sub>	Fall time	—	9.4	—		
E <sub>off</sub>	Turn off Energy	—	200	—	μJ	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V to 12V, R <sub>G</sub> =15Ω, I <sub>D</sub> =60A, Z <sub>FB</sub> =180Ω at 100MHz
E <sub>on</sub>	Turn on Energy	—	663	—		

Notes:

- Dynamic on-resistance; see Figures 18 and 19 for test circuit and conditions
- Equivalent capacitance to give same stored energy as V<sub>DS</sub> rises from 0V to 400V
- Equivalent capacitance to give same charging time as V<sub>DS</sub> rises from 0V to 400V

# TP65H015G5WS

## Electrical Parameters (T<sub>J</sub>=25 °C unless otherwise stated)

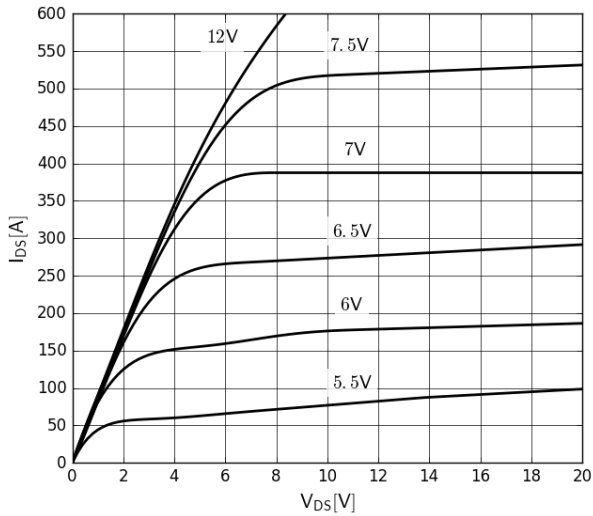
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
<b>Reverse Device Characteristics</b>						
I <sub>S</sub>	Reverse current	—	—	60	A	V <sub>GS</sub> =0V, T <sub>C</sub> =100 °C ≤15% duty cycle
V <sub>SD</sub>	Reverse voltage <sup>a</sup>	—	1.6	—	V	V <sub>GS</sub> =0V, I <sub>S</sub> =60A
		—	1.2	—		V <sub>GS</sub> =0V, I <sub>S</sub> =30A
t <sub>RR</sub>	Reverse recovery time	—	100	—	ns	I <sub>S</sub> =60A, V <sub>DD</sub> =400V, di/dt=1000A/μs
Q <sub>RR</sub>	Reverse recovery charge	—	430	—	nC	
(di/dt) <sub>RM</sub>	Reverse diode di/dt <sup>b</sup>	—	—	3500	A/μs	Circuit implementation and parameters on page 3

Notes:

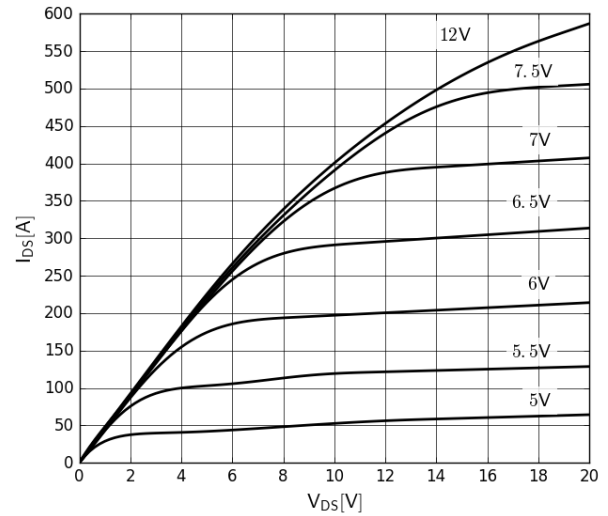
- a. Includes dynamic R<sub>DS(on)</sub> effect
- b. Reverse conduction di/dt will not exceed this max value with recommended R<sub>G</sub>.

# TP65H015G5WS

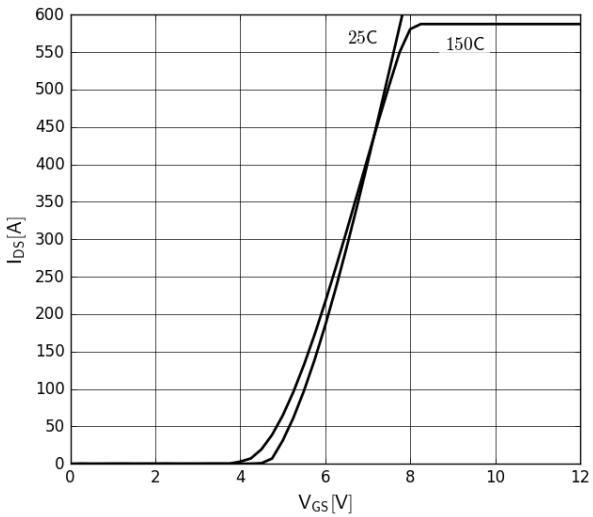
**Typical Characteristics** ( $T_C=25^\circ\text{C}$  unless otherwise stated)



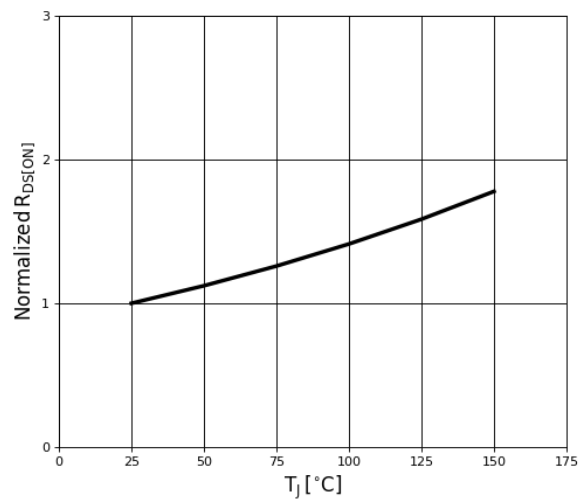
**Figure 1. Typical Output Characteristics  $T_J=25^\circ\text{C}$**   
Parameter:  $V_{GS}$



**Figure 2. Typical Output Characteristics  $T_J=150^\circ\text{C}$**   
Parameter:  $V_{GS}$



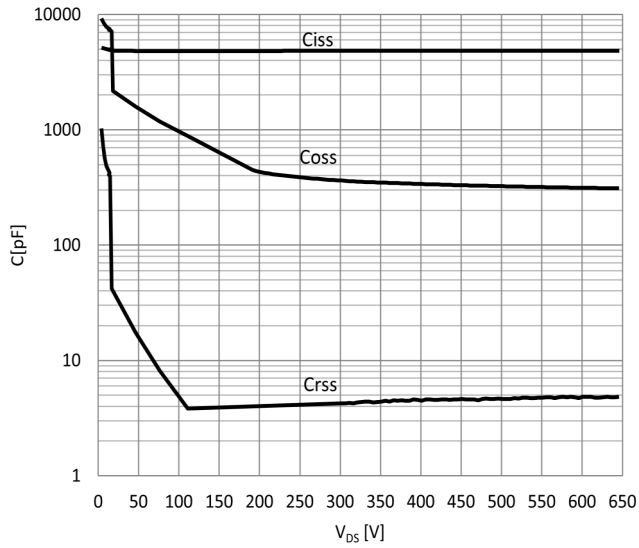
**Figure 3. Typical Transfer Characteristics**  
 $V_{DS}=20\text{V}$ , parameter:  $T_J$



**Figure 4. Normalized On-resistance**  
 $I_D=60\text{A}$ ,  $V_{GS}=8\text{V}$

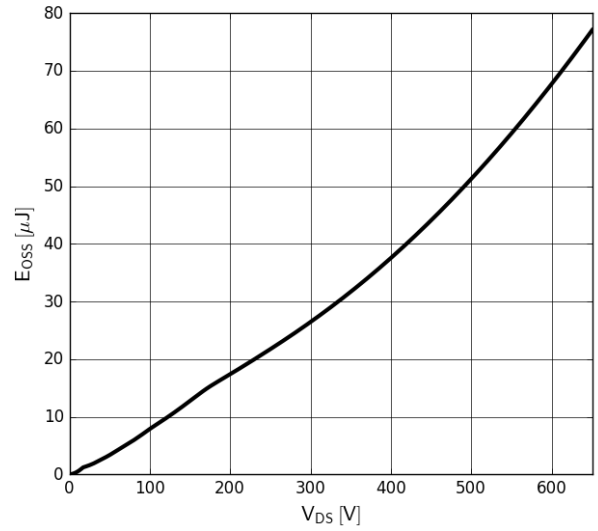
# TP65H015G5WS

**Typical Characteristics** ( $T_C=25^\circ\text{C}$  unless otherwise stated)

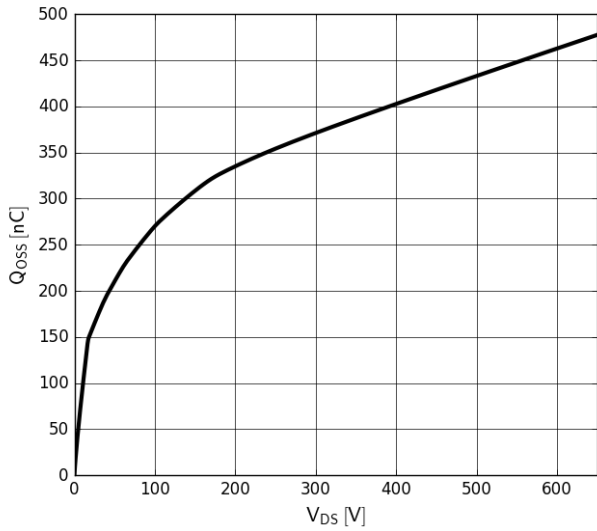


**Figure 5. Typical Capacitance**

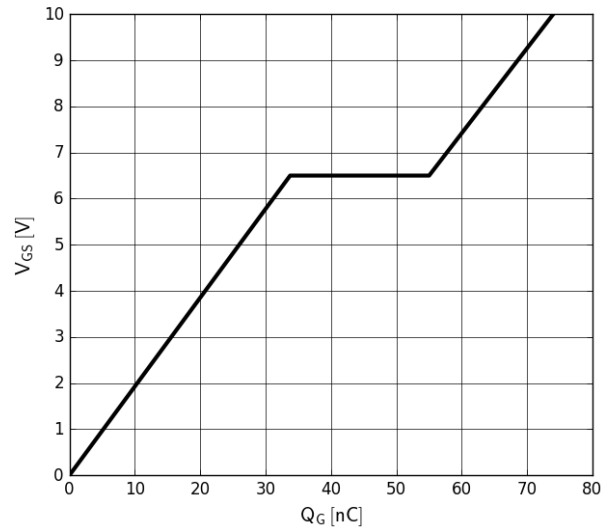
$V_{GS}=0\text{V}$ ,  $f=1\text{MHz}$



**Figure 6. Typical  $C_{oss}$  Stored Energy**



**Figure 7. Typical  $Q_{oss}$**

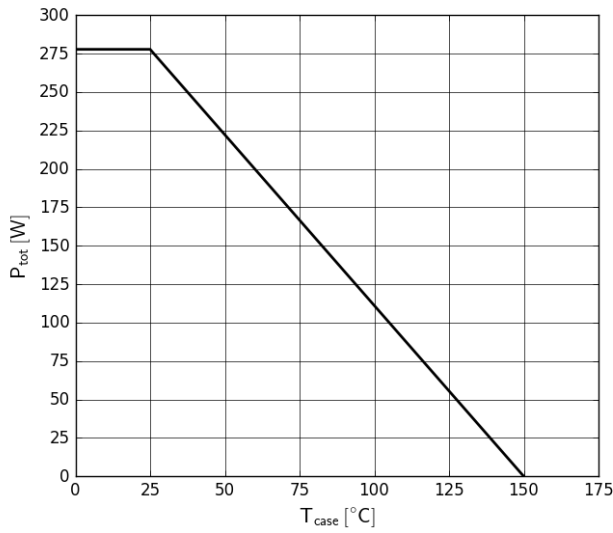


**Figure 8. Typical Gate Charge**

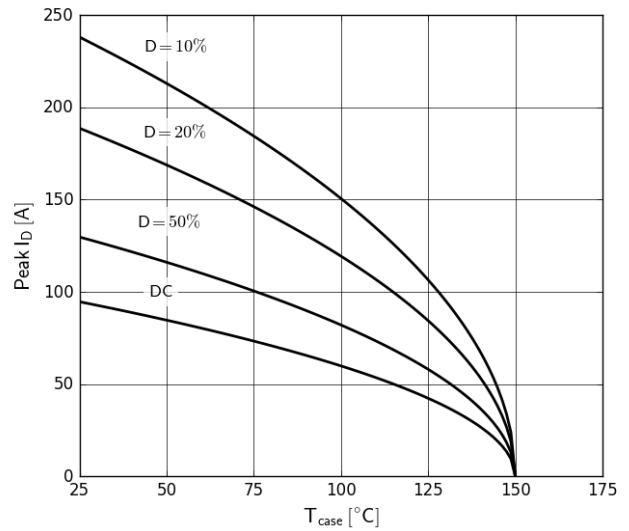
$I_{DS}=60\text{A}$ ,  $V_{DS}=400\text{V}$

# TP65H015G5WS

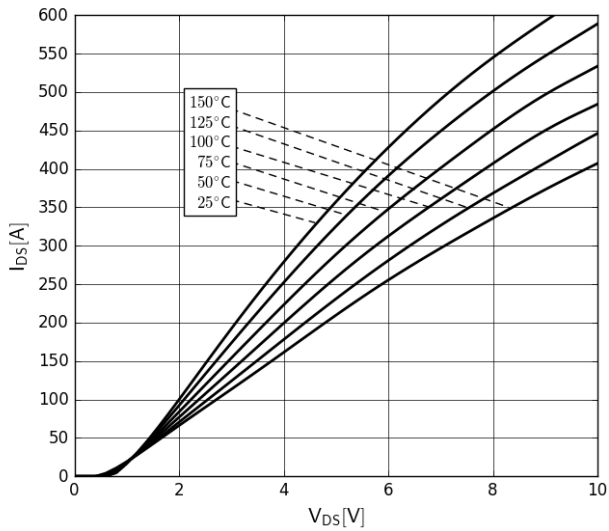
**Typical Characteristics** ( $T_C=25^\circ\text{C}$  unless otherwise stated)



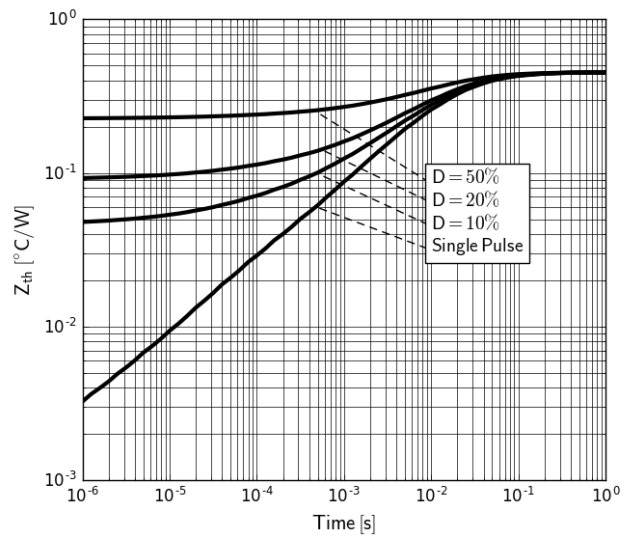
**Figure 9. Power Dissipation**



**Figure 10. Current Derating**  
Pulse width  $\leq 10\mu\text{s}$ ,  $V_{GS} \geq 10\text{V}$



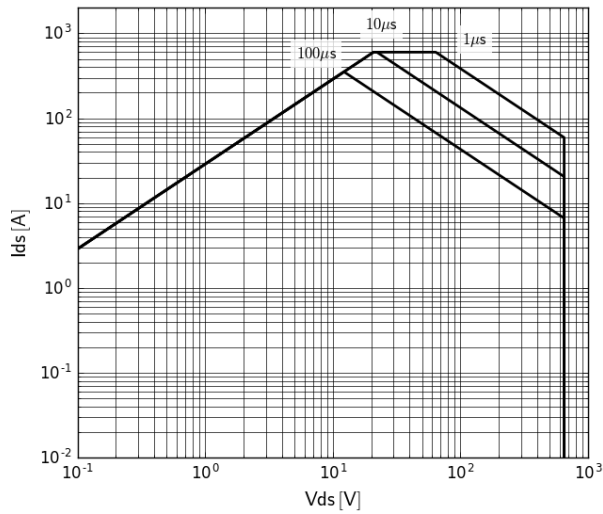
**Figure 11. Forward Characteristics of Rev. Diode**  
 $I_S=f(V_{SD})$ , parameter:  $T_J$



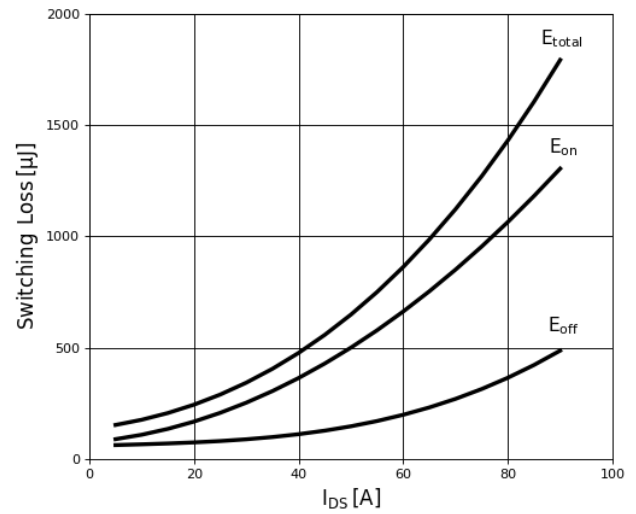
**Figure 12. Transient Thermal Resistance**

# TP65H015G5WS

**Typical Characteristics** ( $T_c=25^\circ\text{C}$  unless otherwise stated)



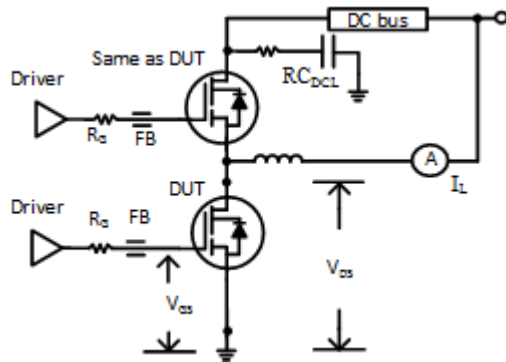
**Figure 13. Safe Operating Area  $T_c=25^\circ\text{C}$**



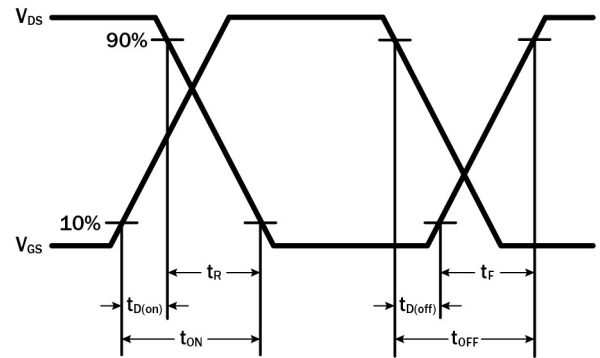
**Figure 14. Inductive Switching Loss  $T_c=25^\circ\text{C}$   
 $R_g=15\Omega$ ,  $V_{DS}=400\text{V}$**

# TP65H015G5WS

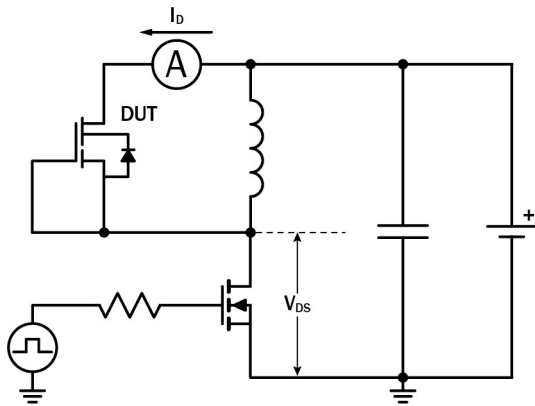
## Test Circuits and Waveforms



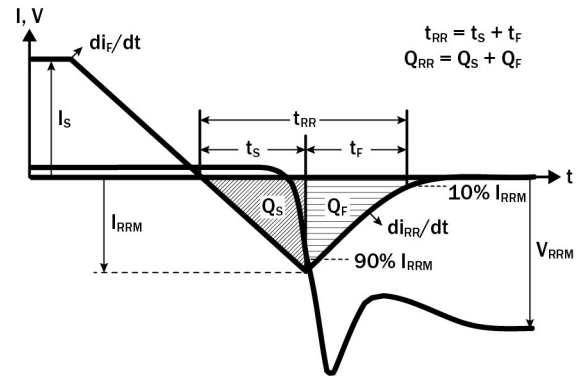
**Figure 14. Switching Time Test Circuit**  
(see circuit implementation on page 3 for methods to ensure clean switching)



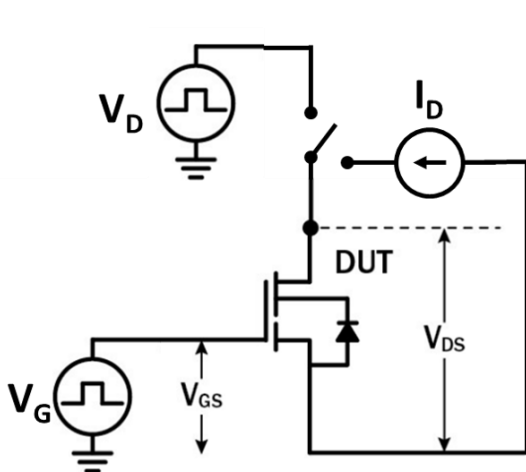
**Figure 15. Switching Time Waveform**



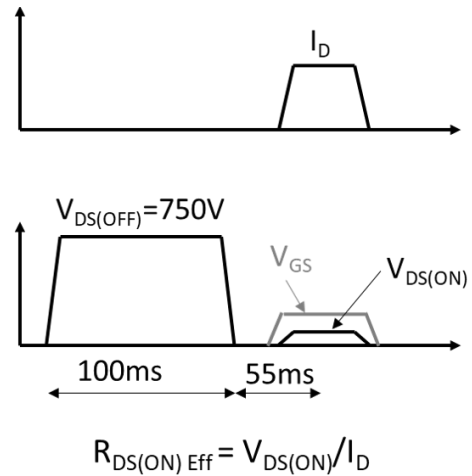
**Figure 16. Diode Characteristics Test Circuit**



**Figure 17. Diode Recovery Waveform**



**Figure 18. Dynamic  $R_{DS(on)eff}$  Test Circuit**



**Figure 19. Dynamic  $R_{DS(on)eff}$  Waveform**

# TP65H015G5WS

## Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

### When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See <a href="#">AN0003</a> : Printed Circuit Board Layout and Probing	

## GaN Design Resources

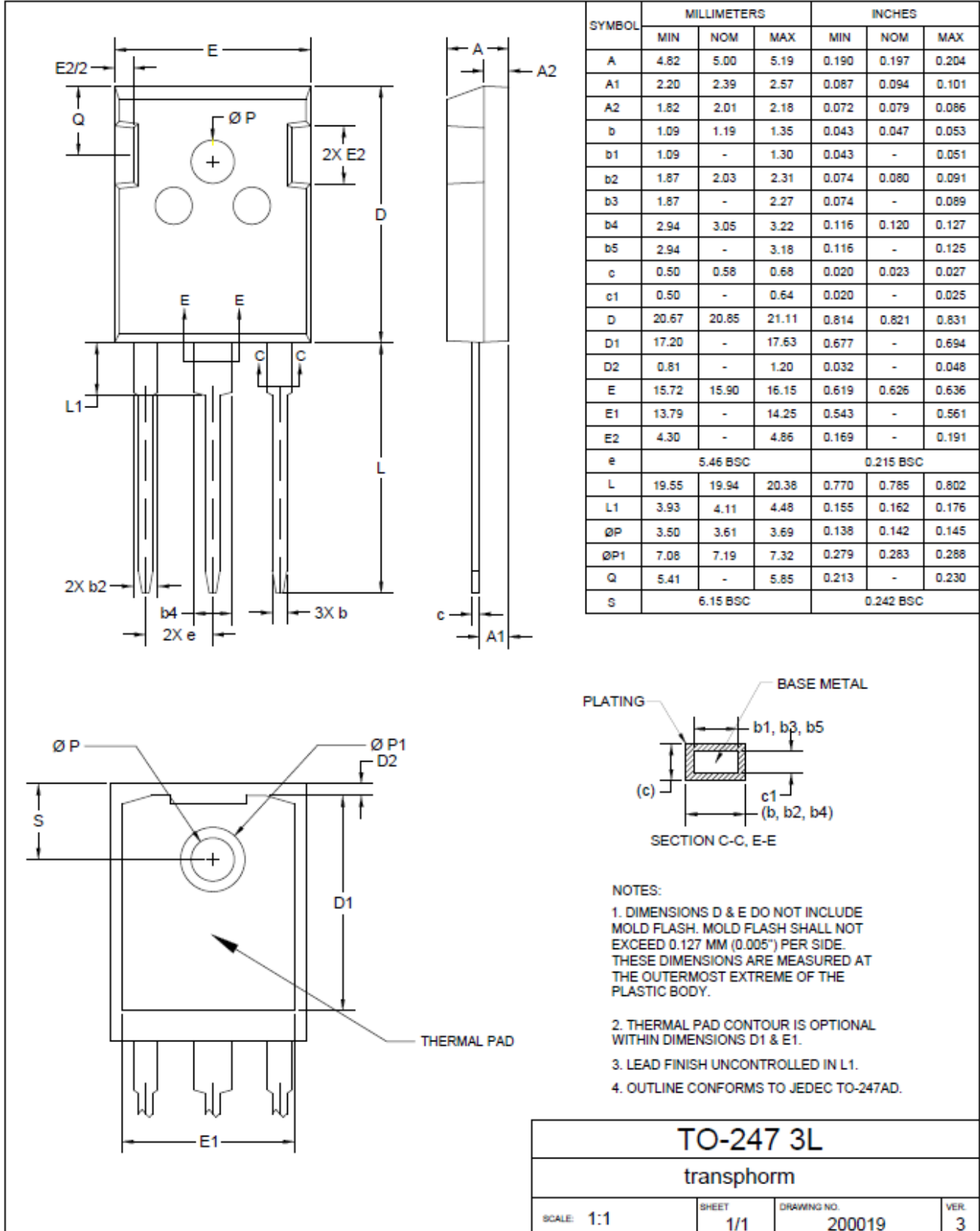
The complete technical library of GaN design tools can be found at [transphormusa.com/design](https://transphormusa.com/design):

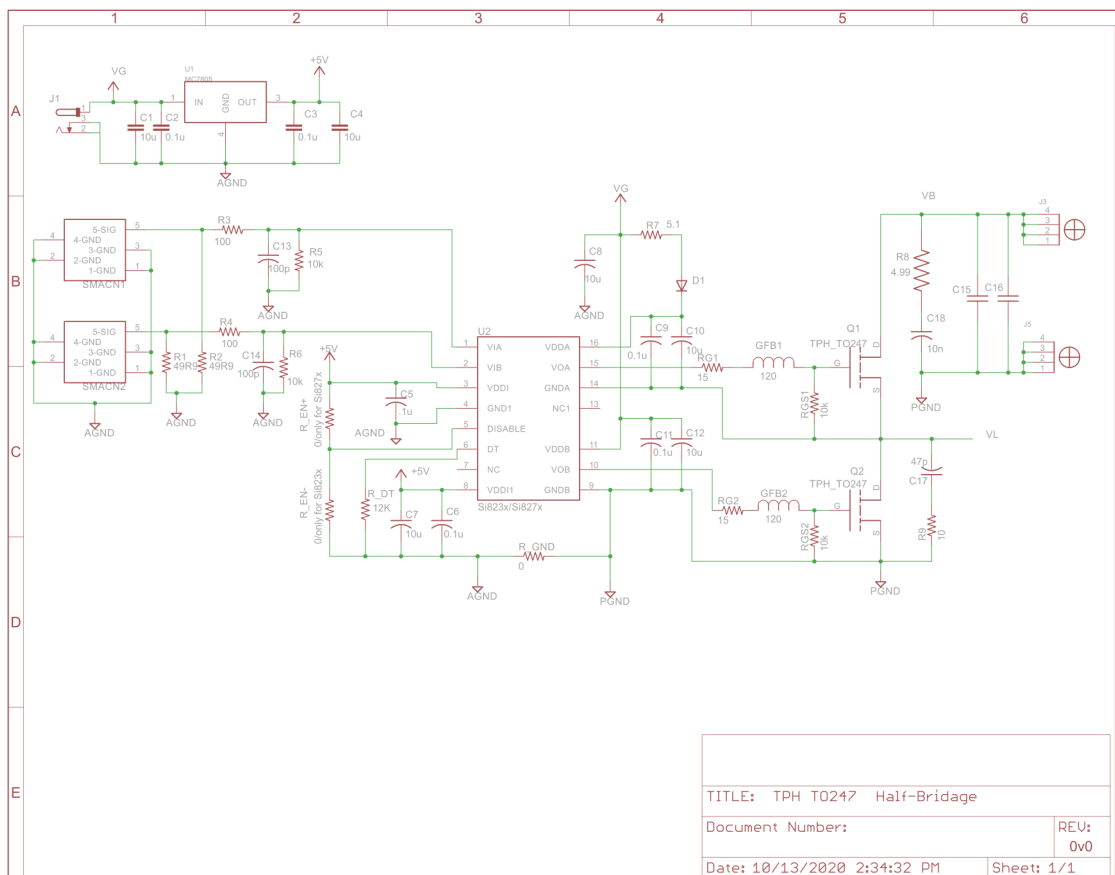
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

# TP65H015G5WS

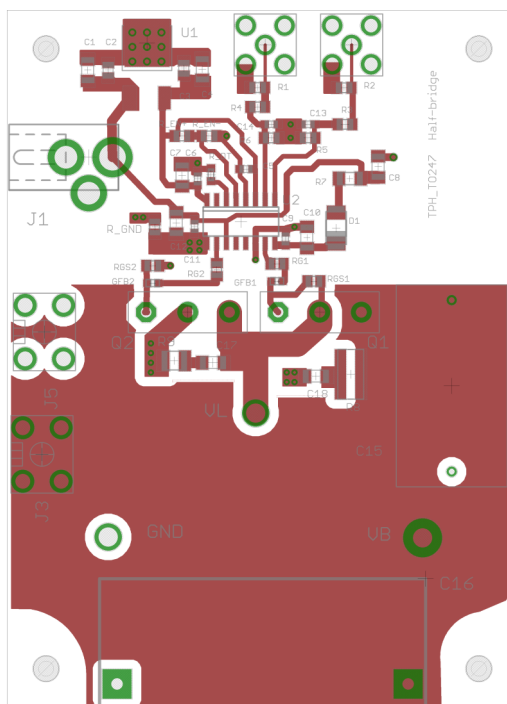
## Mechanical

## 3 Lead TO-247 Package

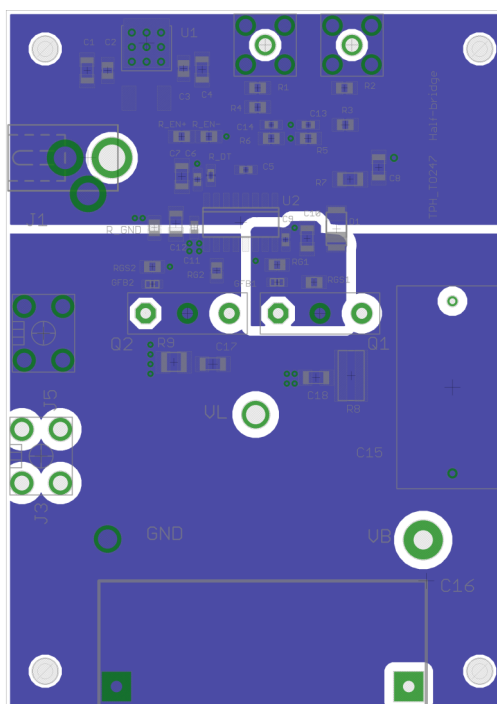




### Half-bridge layout Sample (Top Layer)



### Half-bridge layout Sample (Bottom Layer)



# TP65H015G5WS

## Revision History

Version	Date	Change(s)
0.1	5/25/2020	Preliminary Datasheet
0.2	9/24/2020	Preliminary Datasheet
0.2	02/23/2021	Preliminary Datasheet. Update Figure 18, 19
1.0	07/12/2021	Datasheet complete
1.1	06/29/2022	Updated Page 3 gate driver options and updated C-V curve
1.2	12/30/2022	Added switching loss data on Electrical parameters table and Figure 14
2.0	3/17/2023	Updated 150C Ron as tested