TP65H050G4YS

650V SuperGaN® FET in TO-247 (source tab)

Description

The TP65H050G4YS 650V, 50 mΩ gallium nitride (GaN) FET is a normally-off device using Transphorm's Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

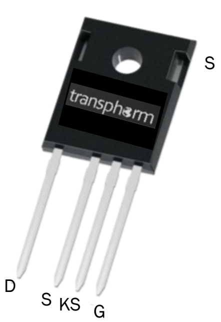
Related Literature

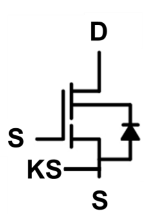
- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing

Ordering Information

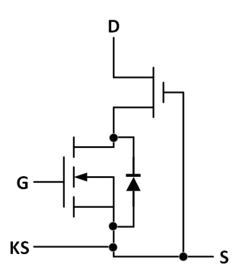
Part Number	Package	Package Configuration
TP65H050G4YS	4 Lead TO-247	Source

TP65H050G4YS
TO-247
(top view)





Cascode Schematic Symbol



Cascode Device Structure

Features

- JEDEC qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - Wide gate safety margin
  - Transient over-voltage capability
- Enhanced inrush current capability
- Very low Q_{RR}
- Reduced crossover loss

Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor

Key Specifications	
V_{DSS} (V)	650
$V_{DSS(TR)}$(V)	800
$R_{DS(on)eff}$ (mΩ) max*	60
Q_{RR} (nC) typ	120
Q_G (nC) typ	16

* Dynamic on-resistance; see Figures 18 and 19

Absolute Maximum Ratings (T_c=25°C unless otherwise stated.)

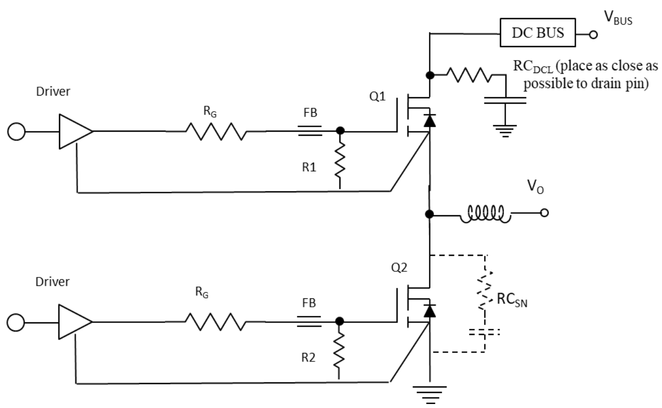
Symbol	Parameter		Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
$V_{DSS(TR)}$	Transient drain to source voltage [a]		800	
V_{GSS}	Gate to source voltage		±20	
P_D	Maximum power dissipation @T_C=25°C		132	W
I_D	Continuous drain current @T_C=25°C [b]		35	A
	Continuous drain current @T_C=100°C [b]		22	A
I_{DM}	Pulsed drain current (pulse width: 10μs)		150	A
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{SOLD}	Soldering peak temperature [c]		260	°C
-	Mounting Torque		70	N cm

Notes:
a. In off-state, spike duty cycle D<0.01, spike duration <30μs, non repetitive
b. For increased stability at high current operation, see Circuit Implementation on page 3
c. For 10 sec., 1.6mm from the case

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	0.95	°C/W
$R_{\Theta JA}$	Junction-to-ambient	40	°C/W

Circuit Implementation



Simplified Half-bridge Schematic (See also on Figure 15)

For additional gate driver options/configurations, please see Application Note AN0009

Layout Recommendations
Gate Loop:

- Gate Driver: SiLab Si823x/Si827x
- Keep gate loop compact
- Minimize coupling with power loop

Power loop: (For reference see page 13)

- Minimize power loop path inductance
- Minimize switching node coupling with high and low power plane
- Add DC bus snubber to reduce to voltage ringing
- Add Switching node snubber for high current operation

Parameter	Symbol	Value
Gate Resistor	R_G	47 Ω
Operating frequency	F_{sw}	50~100 kHz
Gate Ferrite Bead	FB	180 – 270 Ω at 100MHz(d)
Gate-to-source Resistor	R1/R2	10 kΩ
DC Link RC Noise Filter	RC_{DCL}	10nF+ 5Ω]
Switching Node RC Snub-	RC_{SN}	Not Necessary (e)
Gate Driver	Driver	Si8230/Si8274

Note:
d. For every design and layout, a range of ferrite beads (FB) should be evaluated to help suppress any high frequency ringing
e. RC_{SN} (47pF + 5Ω) is needed if

- R_G is smaller than recommendations
- Layout is not optimized
- Requires high current operation

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{DSS(BL)}$	Drain-source voltage	650	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	3.3	4	4.8	V	V_{DS}=V_{GS}, I_D=0.7mA
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	—	-6.2	—	mV/°C	
$R_{DS(on)eff}$	Drain-source on-resistance [a]	—	50	60	mΩ	V_{GS}=10V, I_D=22A
		—	105	—		V_{GS}=10V, I_D=22A, T_J=150°C
I_{DSS}	Drain-to-source leakage current	—	4	40	μA	V_{DS}=650V, V_{GS}=0V
		—	15	—		V_{DS}=650V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=20V
		—	—	-100		V_{GS}=-20V
C_{ISS}	Input capacitance	—	1000	—	pF	V_{GS}=0V, V_{DS}=400V, *f*=1MHz
C_{OSS}	Output capacitance	—	110	—		
C_{RSS}	Reverse transfer capacitance	—	2.7	—		
$C_{O(er)}$	Output capacitance, energy related [b]	—	164	—	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related [c]	—	280	—		
Q_G	Total gate charge	—	16	24	nC	V_{DS}=400V, V_{GS}=0V to 10V, I_D=22A
Q_{GS}	Gate-source charge	—	6	—		
Q_{GD}	Gate-drain charge	—	5	—		
Q_{OSS}	Output charge	—	112	—	nC	V_{GS}=0V, V_{DS}=0V to 400V
$t_{D(on)}$	Turn-on delay	—	40	—	ns	V_{DS}=400V, V_{GS}=0V to 10V, I_D=22A, Rg(on)=47Ω, Rg(off) =39Ω, Z_{FB}=120Ω at 100MHz (See Figure 14)
t_R	Rise time	—	5	—		
$t_{D(off)}$	Turn-off delay	—	40	—		
t_F	Fall time	—	8	—		
E_{off}	Turn off Energy	—	72.7	—	μJ	V_{DS}=400V, V_{GS}=0V to 12V, R_G=47Ω, I_D=22A, Z_{FB}=180Ω at 100MHz
E_{on}	Turn on Energy	—	53.8	—	μJ	

Notes:
a. Dynamic on-resistance; see Figures 17 and 18 for test circuit and conditions
b. Equivalent capacitance to give same stored energy as V_{DS} rises from 0V to 400V
c. Equivalent capacitance to give same charging time as V_{DS} rises from 0V to 400V

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	22	A	V_{GS}=0V, T_C=100°C, ≤25% duty cycle
V_{SD}	Reverse voltage [a]	—	2.2	2.6	V	V_{GS}=0V, I_S=22A
		—	1.6	1.9		V_{GS}=0V, I_S=11A
t_{RR}	Reverse recovery time	—	50	—	ns	I_S=22A, V_{DD}=400V
Q_{RR}	Reverse recovery charge	—	0	—	nC	
$(di/dt)_{RM}$	Reverse diode di/dt [b]	—	—	2500	A/μs	Circuit implementation and parameters on page 3

Notes:
a. Includes dynamic $R_{DS(on)}$ effect
b. Reverse conduction di/dt will not exceed this max value with recommended R_G.

Typical Characteristics (T_C=25°C unless otherwise stated)

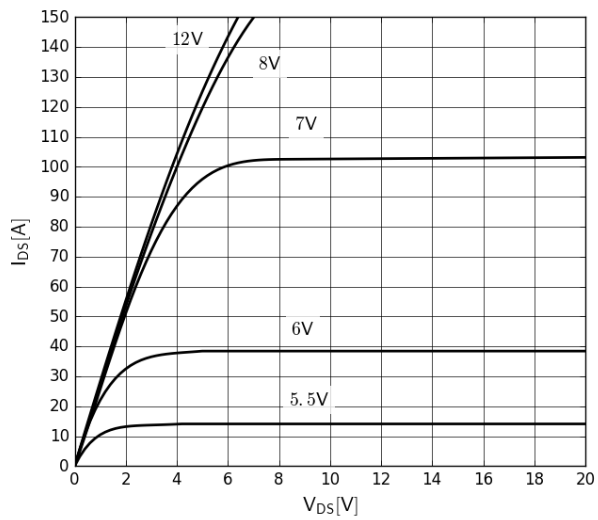


Figure 1. Typical Output Characteristics T_J=25°C

Parameter: V_{GS}

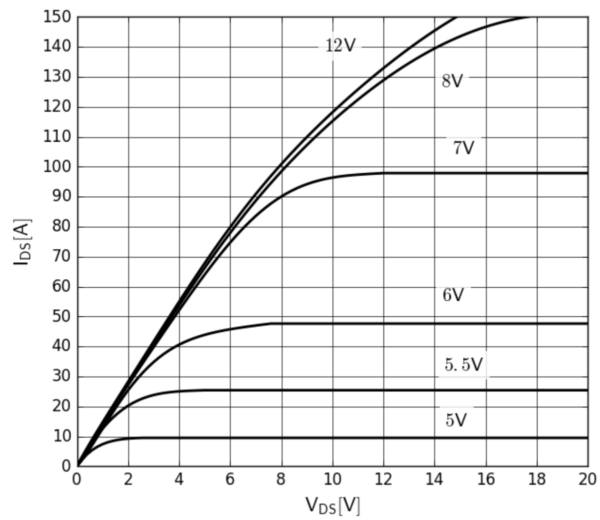


Figure 2. Typical Output Characteristics T_J=150°C

Parameter: V_{GS}

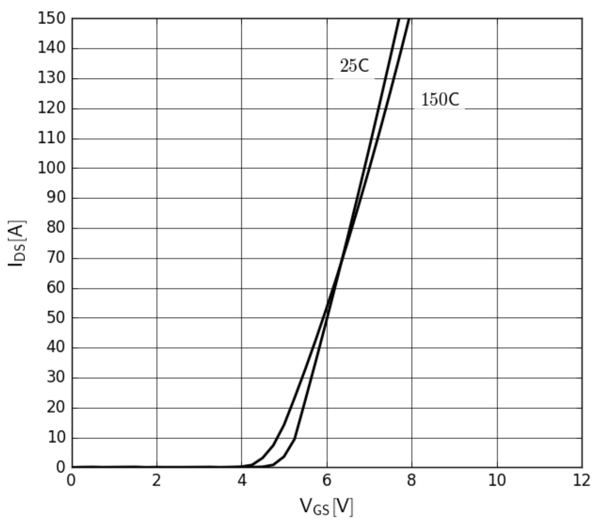


Figure 3. Typical Transfer Characteristics

V_{DS}=20V, parameter: T_J

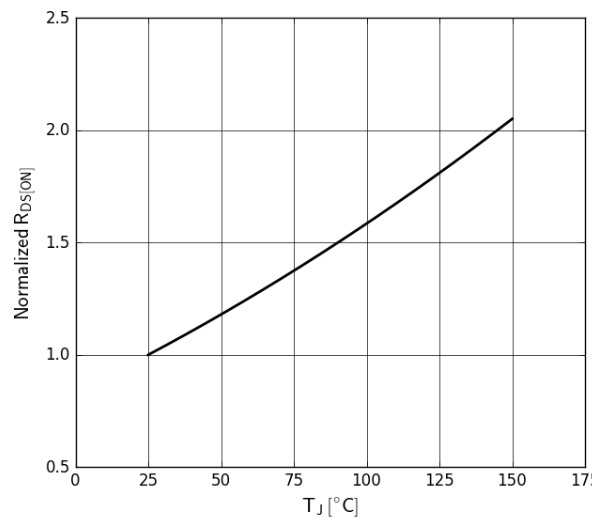


Figure 4. Normalized On-resistance

I_D=22A, V_{GS}=10V

Typical Characteristics (T_C=25 °C unless otherwise stated)

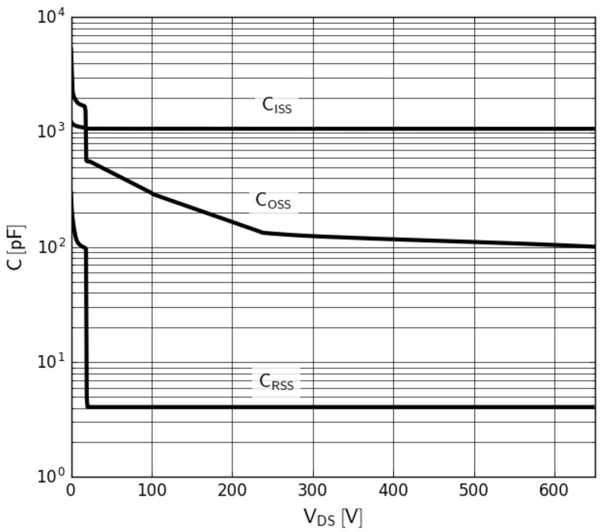


Figure 5. Typical Capacitance
V_{GS}=0V, f=500kHz

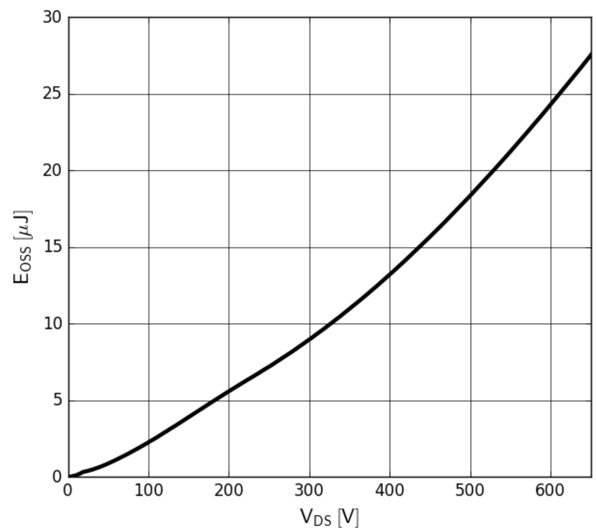


Figure 6. Typical C_{OSS} Stored Energy

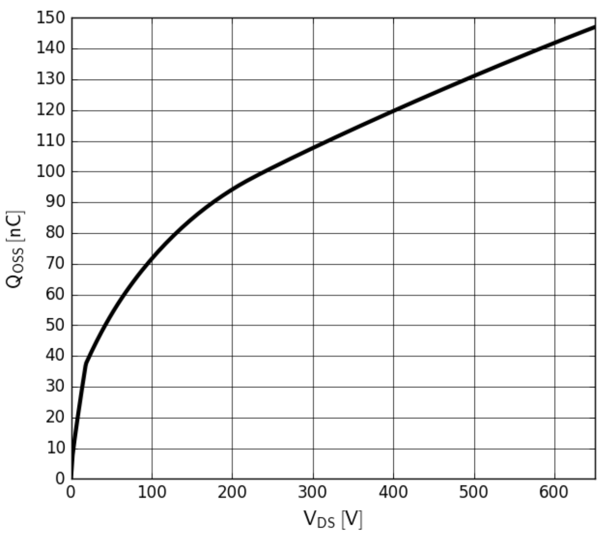


Figure 7. Typical Q_{OSS}

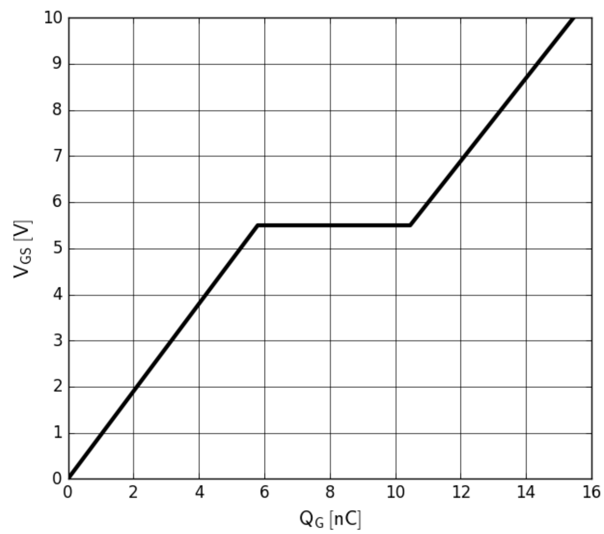


Figure 8. Typical Gate Charge
I_{DS}=22A, V_{DS}=400V

Typical Characteristics (T$_C$=25°C unless otherwise stated)

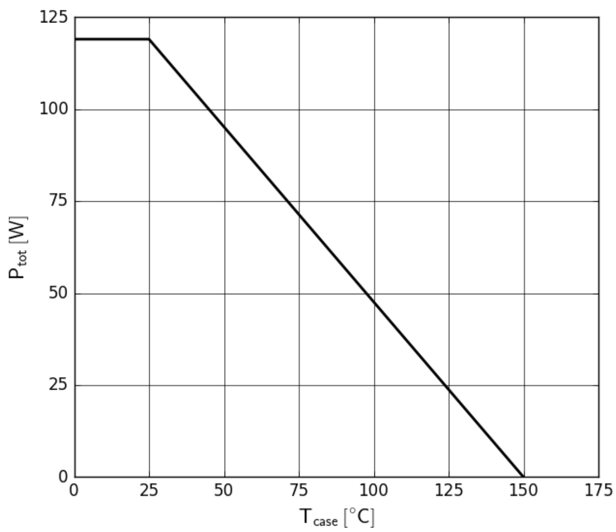


Figure 9. Power Dissipation

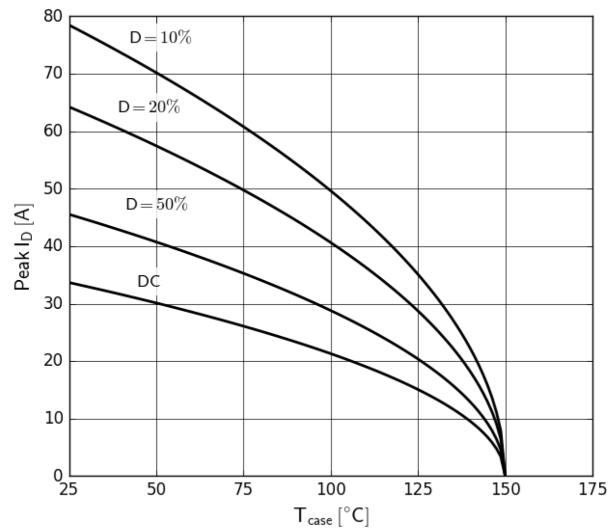


Figure 10. Current Derating
Pulse width ≤ 10μs, V_{GS} ≥ 10V

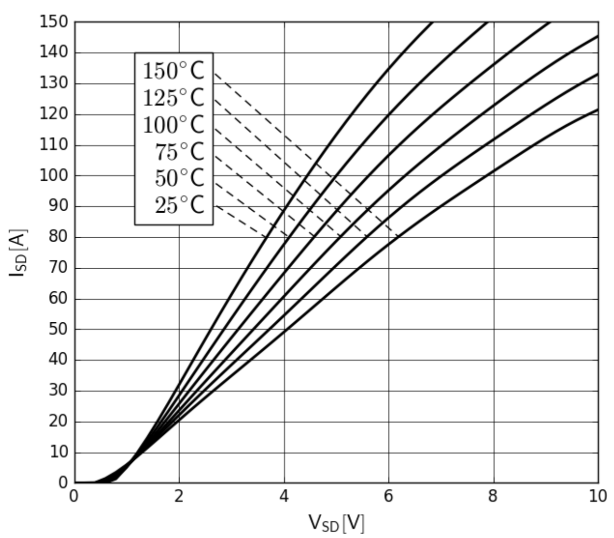


Figure 11. Forward Characteristics of Rev. Diode
I_S=f(V_{SD}), parameter: T_J

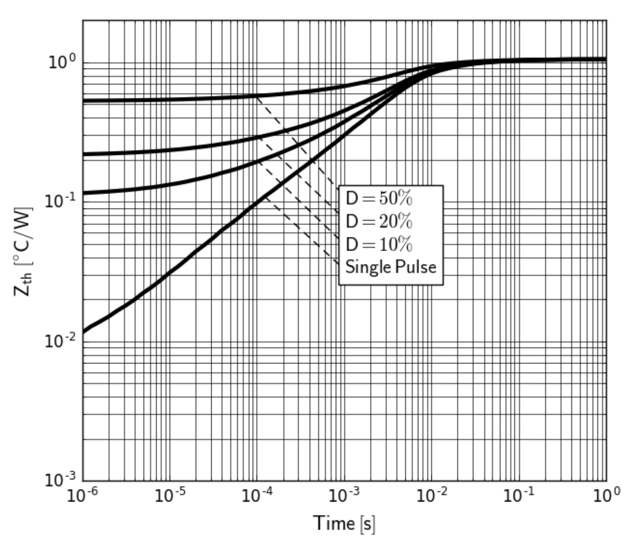


Figure 12. Transient Thermal Resistance

Typical Characteristics (T_C=25 °C unless otherwise stated)

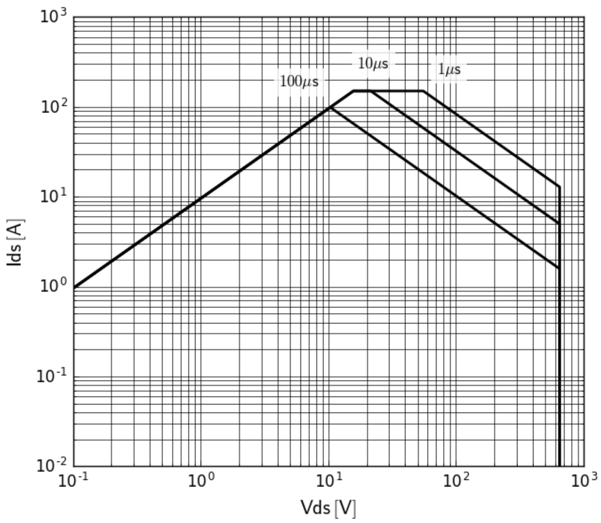


Figure 13. Safe Operating Area T_C=25 °C

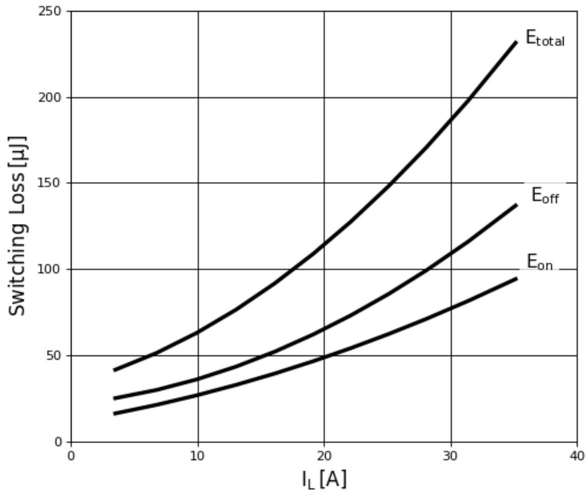


Figure 14. Inductive Switching Loss T_C=25 °C
Rg=47Ω, V_{DS}=400V

Test Circuits and Waveforms

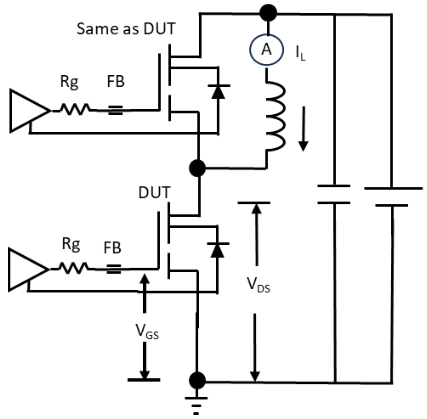


Figure 13. Switching Time Test Circuit
(see circuit implementation on page 3

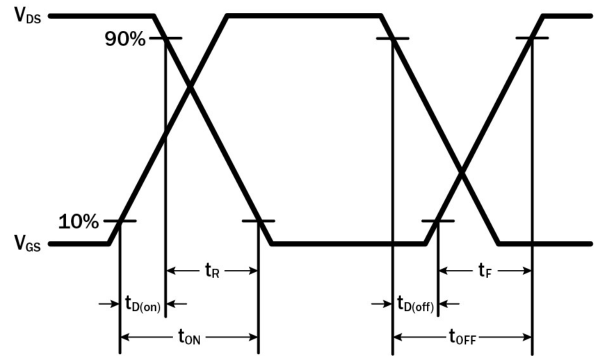


Figure 14. Switching Time Waveform

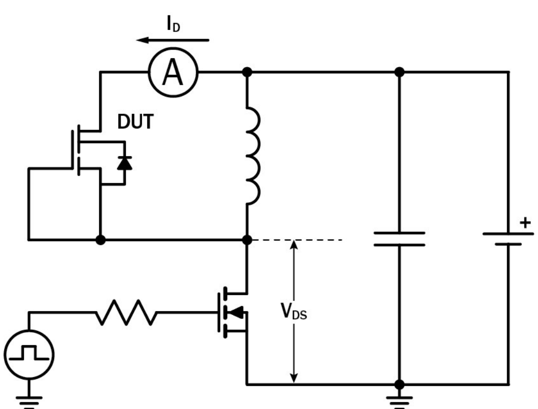


Figure 15. Diode Characteristics Test Circuit

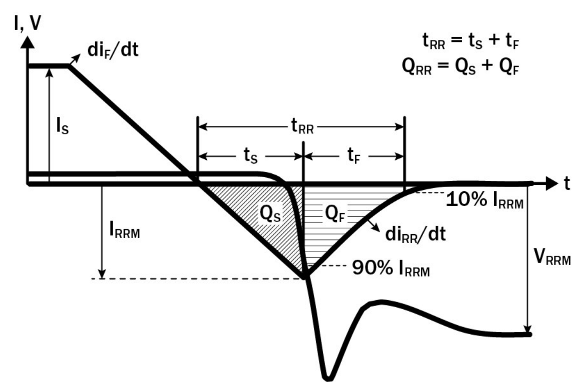


Figure 16. Diode Recovery Waveform

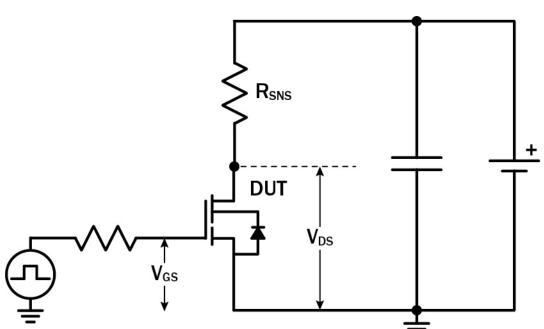


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

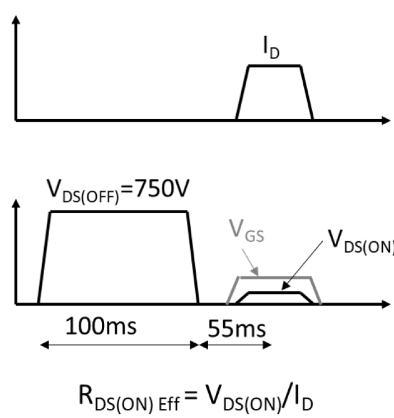


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

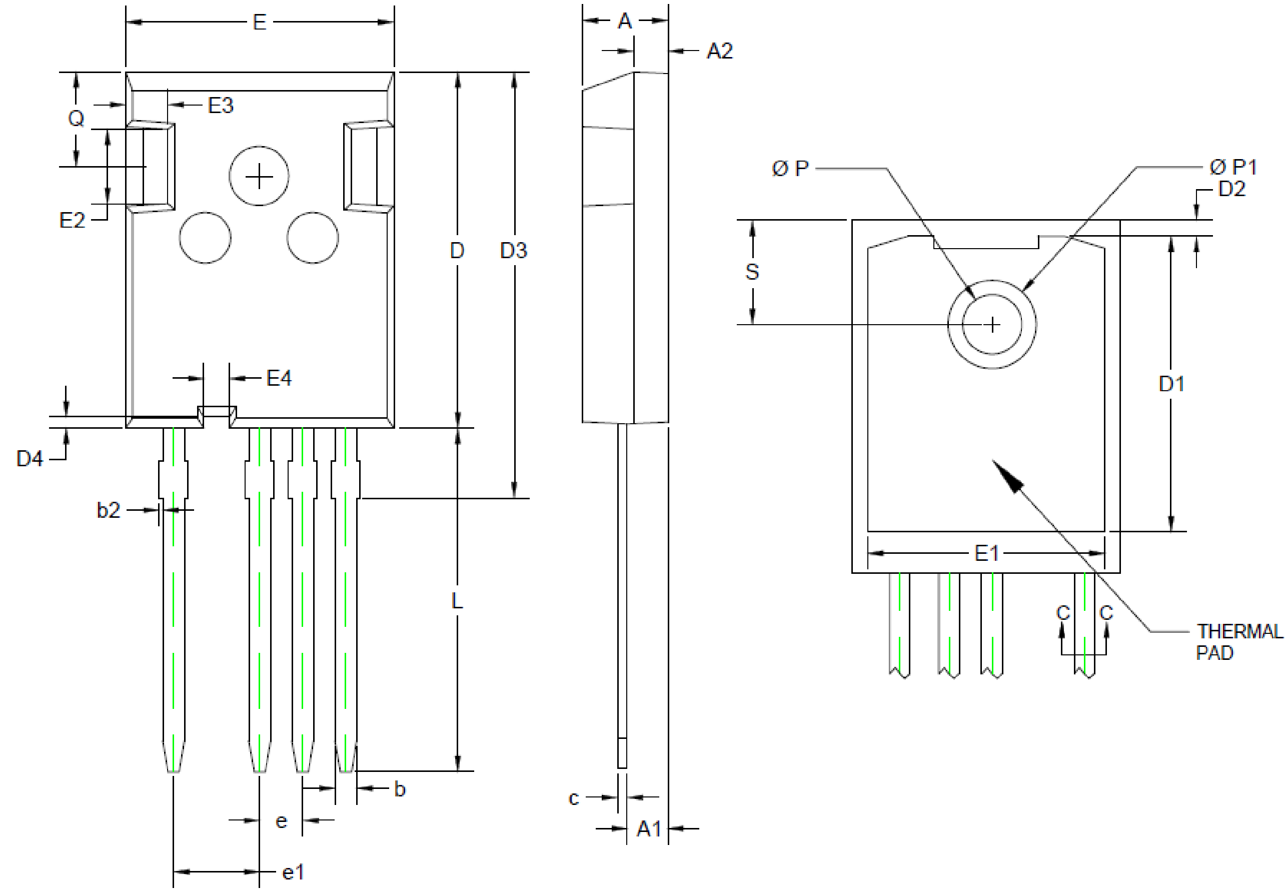
DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

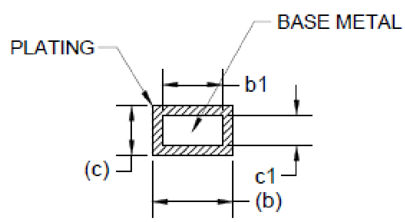
GaN Design Resources

The complete technical library of GaN design tools can be found at transphormusa.com/design:

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Mechanical **4 Lead TO-247 Package**





SECTION C-C

NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.

2. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS D1 & E1.

3. OUTLINE CONFORMS TO JEDEC TO-247AD.

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.90	5.00	5.10	0.192	0.196	0.201
A1	2.31	2.41	2.51	0.090	0.094	0.099
A2	1.90	2.00	2.10	0.074	0.078	0.083
b	1.16	-	1.29	0.045	-	0.051
b1	1.15	1.20	1.25	0.045	0.047	0.050
b2	0	-	0.20	0	-	0.008
c	0.59	-	0.66	0.023	-	0.027
c1	0.58	0.60	0.62	0.022	0.023	0.025
D	20.90	21.00	21.10	0.822	0.826	0.831
D1	16.25	16.55	16.85	0.639	0.651	0.664
D2	1.05	1.20	1.35	0.041	0.047	0.054
D3	24.97	25.12	25.27	0.983	0.988	0.995
D4	0.55	0.65	0.75	0.021	0.025	0.030
E	15.70	15.80	15.90	0.618	0.622	0.627
E1	13.10	13.30	13.50	0.515	0.523	0.532
E2	4.90	5.00	5.10	0.192	0.196	0.201
E3	2.40	2.50	2.60	0.094	0.098	0.103
E4	1.40	1.50	1.60	0.055	0.059	0.064
e	2.44	2.54	2.64	0.096	0.100	0.105
e1	4.98	5.08	5.18	0.196	0.200	0.205
L	19.80	19.92	20.10	0.779	0.784	0.792
P	3.50	3.60	3.70	0.137	0.141	0.146
P1	-	-	7.40	-	-	0.292
Q	5.60	-	6.00	0.220	-	0.237
S	6.15 BSC			0.242 BSC		

TO-247 4L TP65HXXXG4YS

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