TRANSPHORM QUALITY AND
RELIABILITY MANUAL

transphorm

INTRODUCTION TO TRANSPHORM

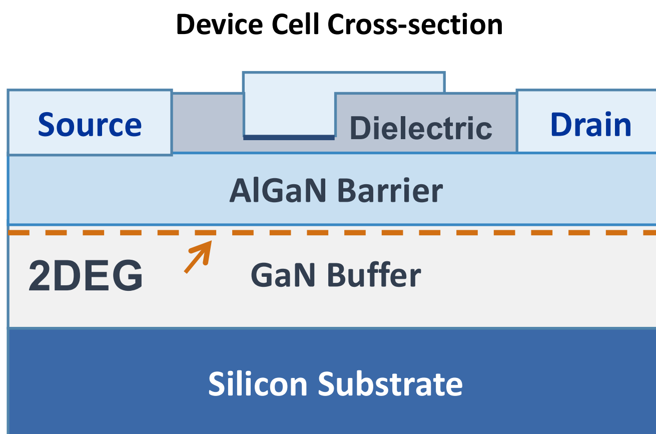
Transphorm, which was founded in 2007, is the world's leading supplier of high-voltage gallium nitride (GaN) based components that are used in a wide array of power conversion applications.

Power conversion is the transformation of electricity from one form to another (such as DC to AC in solar power) and is performed most efficiently and economically when circuits are switched at high frequencies.

Transphorm's high-voltage GaN devices switch at far higher frequencies and with much lower losses than traditional materials such as silicon. This superior material, coupled with innovative circuit design, enables the world's most efficient, most compact, and most cost-effective power conversion technology.

Transphorm designs and manufactures power modules and discrete GaN components based on its patented technology at its headquarters in Goleta, California and supports its customers from its offices in the US, China, Asia, and Europe.

Transphorm's Quality Policy states: **Transphorm is committed to providing products that will enable our customers to deliver best-in-class performance to their customers**. The policy emphasizes our focus on not just the products that we design and manufacture, but also on how they will be used by our customers in their application. Transphorm's designers and applications engineers work closely with customers to ensure that our products exceed our customer's expectations. We win when our customers win.



Transphorm's markets demand and expect the highest levels of quality and reliability. While there are great rewards for those who are willing to implement new technology, there are perceptions of risk that must be overcome. Transphorm recognized very early that proof of our device reliability and quality would be required to accelerate the adoption of its technology.

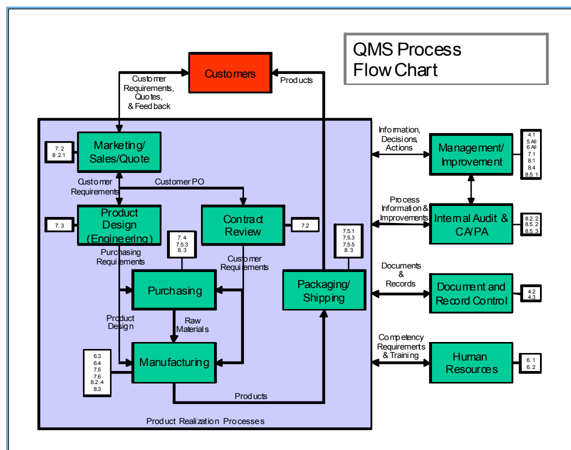
Transphorm has created the business infrastructure and a Quality Management System to ensure the quality of its products and has invested a majority of our engineering resources into proving our products' reliability. Transphorm was the first to JEDEC-qualify 600V GaN products and has more experience manufacturing qualified high-voltage GaN products than anyone in the world.

TRANSPHORM QUALITY MANAGEMENT SYSTEM

Transphorm designs and manufactures ultra-efficient power transistors and modules that can eliminate more than 50% of all electric conversion losses. From HVACs to hybrids and servers to solar panels, Transphorm enables significant energy savings across the grid. To ensure that Transphorm's products meet our customers' highest expectations for quality and reliability, Transphorm has established a Quality Management System that has been certified to the ISO9001:2008 standard.

The scope of the Quality Management System (QMS) is:

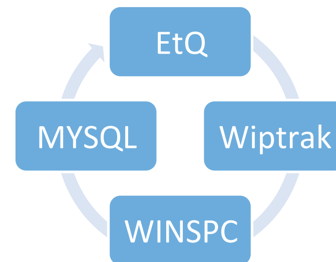
The Design, Development, Manufacture and Sales of GaN power conversion products for Industrial, Consumer, Medical, and Defense applications



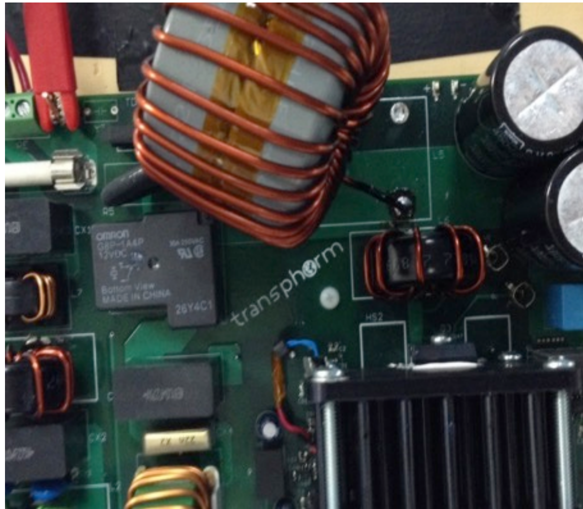
Transphorm has integrated a lean six sigma philosophy as part of its QMS. Lean methodology is focused on streamlining of operations and the elimination of waste while six sigma emphasizes reducing variation and the elimination of defects and mistakes.

At the heart of Transphorm's lean six sigma program is a sophisticated information management system that supports statistical process control, corrective and preventative actions, failure analysis, lot travelers, and production histories.

EtQ is a cloud based document database system that is used for document control, corrective actions, preventative action, RMAs, calibration tracking, and other key functions that support the QMS. Wiptrak is our online manufacturing execution system (MES) that is used to generate process travelers, track process control data, and works in process (WIP). WINSPC is an online statistical process control system (SPC) that supports the standard array of control charts, which is integrated into our MYSQL database system. Our MYSQL database system is the repository of all of our product quality, reliability, and test data. We also support an extensive set of custom designed, proprietary quality and engineering analysis tools, along with the ability to export data for off line analysis using Excel, JMP, MATLAB or R software.



PRODUCT RELIABILITY



From its inception Transphorm has performed comprehensive reliability testing of its products and has achieved industry firsts in qualifying 600V and 650V GaN products for the marketplace. Transphorm has continued to expand application-relevant testing to determine quality, FIT levels, and long-term reliability of its products.

Transphorm begins with standard JEDEC qualification testing and performs additional stress testing to commercialize its GaN power devices to ensure that the quality of GaN devices will meet customer expectations for reliability. The JEDEC tests were originally developed on silicon technology and it is appropriate to understand the assumptions that underlie the tests and determine the level of risk mitigation that the test data provides for power GaN products. Transphorm's testing goes beyond the minimum requirements of JEDEC, by running tests on a much larger number of devices than the minimum required. We use this data to derive the projected failure in time (FIT) rates for our GaN devices.

Beyond initial quality, we use highly-accelerated stress testing to predict how long the devices will last under a wide variety of use-case scenarios. High temperature testing is used to predict device lifetimes due to temperature-related degradation as the devices are passing current at low voltages. The high-voltage rating of the parts is related to the blocking portion of operation, so high field testing is used to predict device lifetime where current is being blocked. Additionally, the transition between the two operating conditions is tested by operating the devices for extended periods of time at maximum operating conditions.

Bathtub curve and reliability

The bathtub curve is typically used to represent the three phases in a product's reliability history. An "infant mortality phase" is characterized by relatively large numbers of early failures with a decreasing frequency. The flat part of the bathtub curve represents relatively small numbers of failures at a constant frequency, and the wear-out period starts with a relatively small numbers of failures, whose frequency increases over time.

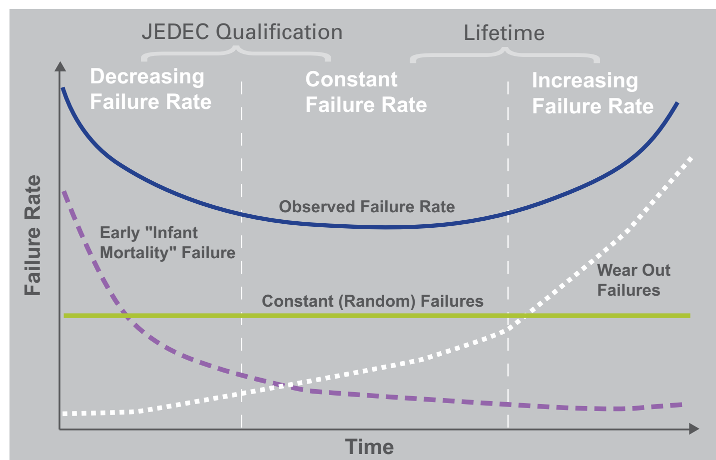


Figure 1. Reliability lifecycle illustrated using a bathtub curve

JEDEC Qualification

JEDEC testing typically utilizes relatively large numbers of devices and applies a fairly modest level of stress to those devices. The tests are designed to give a lot of information about infant mortality and a limited amount of information about the constant failure rate portion of the bathtub curve. The wear-out portion of the bathtub curve will be addressed in the section on life testing on page 9. Table 1 illustrates the tests that comprise Transphorm's typical JEDEC qualification test set.

Table 1. JEDEC qualification test results for Transphorm's 600V products

Test	Symbol	Conditions	Sample	Pass criteria
High Temperature Reverse Bias	HTRB	TJ=150°C V_{DS} = 480V 1000 HRS	3 lots 77 parts per lot 231 total parts	0 Fails
Highly Accelerated Temp and Humidity Test	HAST	130°C 85% RH 33.3 PSI Bias = 100V 96 HRS	3 lots 77 parts per lot 231 total parts	0 Fails
Temperature Cycle	TC	-55°C / 150°C 2 Cycles / HR 1000 Cycles	3 lots 77 parts per lot 231 total parts	0 Fails
Power Cycle	PC	25°C / 150°C ΔT = 100 7500 Cycles	3 lots 77 parts per lot 231 total parts	0 Fails
High Temperature Storage Life	HTSL	150°C 1000 HRS	3 lots 77 parts per lot 231 total parts	0 Fails

In addition to these electrical tests, there are the standard mechanical tests for die attach and bond wire strength typical for any semiconductor product. By passing this suite of tests we have statistical assurance that our products are free from any of the typical defects that can have a negative impact on short- to medium-term reliability.

Given that we understand that JEDEC qualification is focused on the first two phases of the bathtub curve (we address the wear-out phase later in this paper) we can examine Transphorm's standard and extended qualification results.

Defect density and sample size

The more parts that we sample in any qualification test, the more likely we are to sample a part that fails. The industry-standard test, which has been influenced very heavily by automotive quality requirements, is to test three lots with 77 parts in each lot and passing the test with zero failed parts (3 x 0/77) from a total sample size of 231. This testing scheme satisfies the <3% Lot Tolerance Percent Defective (LTPD) quality level as per JESD47 and all Transphorm products must meet this standard before being released to production.

How sensitive is the standard test? One way to look at the sensitivity of any sampled test is to plot its operating characteristic (OC) curve (Figure 2), which shows the probability of passing the test (Pa) vs. the actual number of defective parts (Do).

The first curve (blue) demonstrates that in order to have a better than 95% chance of passing the standard JEDEC test, defect levels need to be below 0.022% or the probability of passing the test drops rapidly.

While this standard has served the semiconductor industry well for gating the entry of products into the field, a new product has a reasonable chance of passing at an unacceptably high defective rate. It has become common practice to run larger samples over an extended period of time to gain a better understanding of defective levels and generate better confidence that the defective levels are low.

Transphorm has completed HTRB testing on over 2000 parts for 1000 hours without failure.

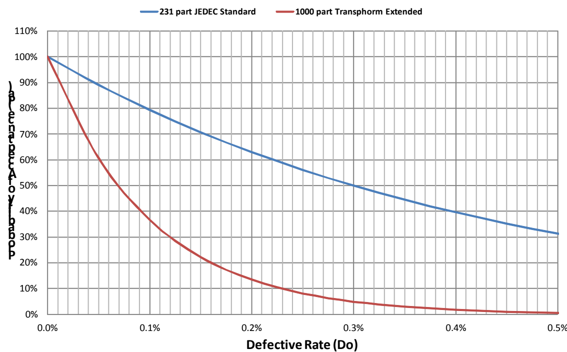


Figure 2. OC curve for 231 part sample plan (JEDEC standard) vs. 1000 part plan (Transphorm extended)

Transphorm continues to sample parts from its production line. As of today, over 2000 parts have been tested through High Temperature Biased (HTRB) for 1000 hours without failure. The red curve shows the OC curve for this sample plan. By testing many lots over an extended period of time Transphorm tests the intrinsic capability of its devices and also tests the stability of the production operation over time. The 2000 parts were sampled in batches of ~50 parts in each lot during the course of 12 months of production time. To have a 95% probability of passing that test, the defect levels need to be below 0.003%, as shown by the red curve. This represents more than an order of magnitude improvement in quality over the standard JEDEC qualification scheme. Transphorm is committed to perpetual reliability testing of its products and is continuing to test. Transphorm's extended samples are large enough to detect very low levels of defects and continuous testing and improvement will help ensure high quality. JEDEC qualification alone does not directly predict field failure rates. We need to look at FIT rate calculations for GaN technology and compare it against silicon technology to understand the relative risk of field failure of a GaN device vs. a silicon device.

FIT calculations

Failures in Time (FIT) rate calculations (failures per billion device hours) is a standard method for predicting field failures of new devices and Transphorm utilizes the method defined in the JEDEC Standard JESD85. The FIT rate calculation is widely used to estimate field failure rates. Because this is a forecast and not an actual measure of field failure rates, there is some statistical uncertainty applied to the calculations. We use a 60% confidence limit which is common industry practice and will enable us to compare GaN with silicon.

The JEDEC methodology assumes a constant rate of failure, which should be representative of the "flat" part of the bathtub curve. Temperature-acceleration is utilized to trigger failures at an accelerated rate. Arrhenius behavior is assumed and that the probability of failure follows a chi-squared distribution. We will utilize the 2000 part extended qualification sample to estimate the FIT rate.

The activation energy (Ea), expressed in eV, is a key factor for determining FIT rates. For the moment we are going to treat this as an unknown variable, though later in this paper we will shed some light on what value the activation energy should take. For the purposes of this study we will assume Tj = 90°C. The voltage applied is 80% of rated Vds, so no voltage acceleration is assumed in the calculation. Failures will solely be driven by temperature acceleration and their rate described by the Arrhenius equation. Our sample size (ss) is 2000, duration (t) 1000 hours, Tstress = 150°C. λ60%CI represents the FIT rate at 60% confidence interval. χ%CI,2f+22 represents the chi-square distribution at 60% confidence interval for number of failures (f) = 0.

Acceleration Factor = AF = $\exp\left[\left(\frac{E_A}{k}\right)\times\left(\left(\frac{1}{T_{use}}\right)-\left(\frac{1}{T_{stress}}\right)\right)\right]$

FIT Rate @ 60% CI = $\lambda_{60\%CI} = \chi^2_{\%CI,2f+2} \times 10^9 \div (2 \times t \times ss \times AF)$

Figure 3 is a graph that shows the relationship between FIT and Ea which shows that as Ea of the failure mechanism increases, the FIT rate decreases. This makes intuitive sense: the more energy it takes to activate the defect mechanism, the longer the product will survive in the field before the defect causes a failure. The lower the FIT rate, the higher the reliability of the device, and the fewer field failures that can be expected. Our own studies indicated Ea = 1.84 eV for GaN as explained later. The FIT rate asymptotically approaches zero at Ea of 1.84 eV.

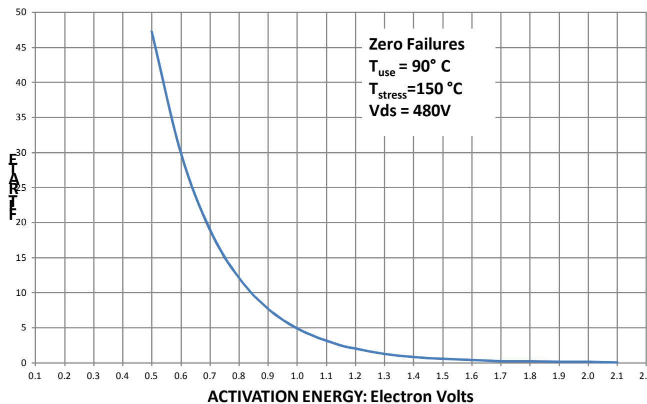


Figure 3. FIT rate calculation 60% confidence interval 2000 part sample, 1000 hours, 2 x 10^6 device-hours

A review of typical activation energies (Failure Mechanism and Modes for Semiconductor Devices – JEP122) shows that many of the documented activation energies of failure modes encountered in semiconductor products have activation energies of approximately 1eV. What this means in a practical sense is that something "else" other than the GaN chip itself will be more likely to fail in the field. Die attach, wire bonds, electro-migration or environmental stress are far more likely to contribute to early field failures than defects in the GaN device.

The inherent reliability risk in GaN products are certainly no greater than for silicon products and one could argue that it is actually less because the high activation energy is related to the wider bandgap of GaN.

One could make the argument that JEDEC testing, because it was developed for silicon, is not giving us an accurate picture of the FIT rates because it doesn't stress the part enough. This is a true statement, but it is also true that JEDEC testing predicts that early life or infant mortality field failures from GaN device are unlikely. It is not unreasonable for us to predict a FIT rate of 5, assuming an activation energy of approximately 1eV, (which represents a weighted average of package and material related failure activation energies). Clearly as we need to be able to predict lifetime in the field, and JEDEC type testing does not give us all the resolution that we need, thus more aggressive accelerated life testing becomes Transphorm's methodology of choice, which we will address next.

High temperature switching operation test

During normal operation, the devices are exposed to many of the JEDEC test conditions simultaneously. High temperature operating life test (HTOL) mimics hard-switching conditions in applications and provides a window into possible interactions affecting reliability. We ran the test on standard parts operating as the main switch in a boost converter. The devices were run at 175°C junction temperature, which is higher than the 150°C reported in the data sheet.

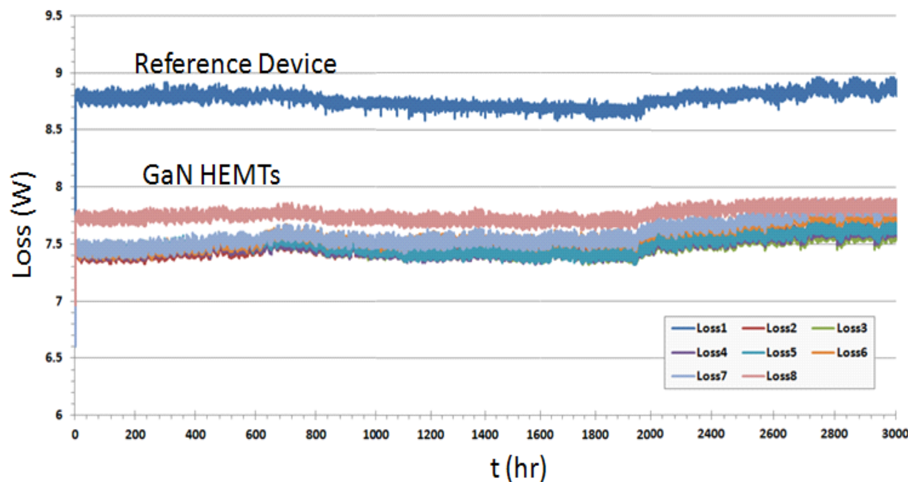


Figure 4. Loss plot for HTOL of seven 600V-rated GaN-on-Si HEMT switch and a reference device to 3000 hours at Tj=175°C. Each device operated in a boost converter at 300kHz with a boost ratio 200V:400V, 410W output power

The higher temperature provides a minor acceleration of the test, but higher temperatures result in the degradation of external components thereby limiting the maximum junction temperature to 175°C. Figure 4 shows conversion loss of the devices over the life of the HTOL. Degradation of the solder contacts and external components in the circuit are the reasons for the increase in conversion loss after 2000 hours and the devices showed no significant change in performance when measured after the HTOL. While this test does not predict lifetime, the GaN devices are robust for extended times at the maximum rated temperature in actual operating conditions.

Product life testing (wear-out testing)

The predicted lifetime or point that the parts will begin to fail at an increasing rate due to aging, is the last region shown in Figure 1. Lifetime projections which depend on understanding and modeling the wear-out process are based upon accelerated testing to failure. The operating conditions of a power switch allow for separation of the major stress factors. In the off-state, the device is blocking a large voltage across the switch with no current flowing in both normal operation and in accelerated voltage testing, allowing for high field testing and lifetime projections without the complications of current and/or temperature extremes. In the on-state, the device is conducting current with a small voltage across it that is similar at both nominal and elevated temperature operation needed for lifetime predictions. The combined understanding from on-state and off-state testing provides confidence that the wear-out predictions are accurate.

Temperature acceleration

We have used temperature-accelerated testing to project on-state lifetimes to be >1 x 10^8 hours. Temperature acceleration is the most common method of projecting device lifetime in III-V semiconductors. The tested devices were parts from standard production runs and the parts were operated in the on-state with a constant current. This maintained constant power dissipation and therefore constant device temperature. Three sets of devices were run at separate high temperatures to provide the physical understanding and lifetime projections based on temperature-related degradation.

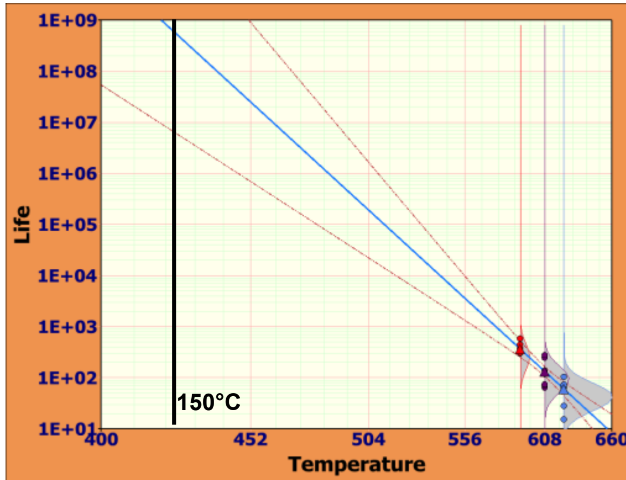


Figure 5. Arrhenius plot showing MTTFs for the three temperatures (in °K) and lifetime extrapolation including 90% confidence limits

Figure 5 shows failure times plotted on a graph of log time vs. 1/temperature in Kelvin (Arrhenius plot). Each set of devices is represented by a mean time to failure (MTTF) point (triangle) or the point at which 50% of the devices are failed. A line is fitted to the MTTF points. The slope of the line provides the physical understanding of the degradation mechanism, through the activation energy. In our case Ea is 1.84eV which is in good agreement with the values reported in the literature. The line also predicts the lifetime at use-temperatures such as 423°K (150°C) which is >1 x 10^8 hours.

The statistical validity is demonstrated both by the range of the failure points and by the 90% confidence limits shown by the dashed lines. The small range of values around the MTTF point (especially for such relatively large devices) gives us confidence that the expected failure mode is being represented. The lower limit of that range is still >1 x 10^6 hours or >100 years at 150°C.

Voltage acceleration

Transphorm was the first to report a GaN high field related lifetime of >1 x 10^8 hours at 600V. High voltages can be a significant reliability concern but Transphorm's device design has limited the electric field strength to levels similar to those seen in RF GaN high electron mobility transistor (HEMT) devices. RF GaN HEMTs have been reported on extensively and successfully used in highly reliable, high-volume production systems for over ten years. Transphorm's standard 600V production parts (GaN HEMTs cascoded with Si FETs) were used for the high field lifetime testing. Three sets of devices were biased in the off-state at high drain voltages of 1050V, 1100V, and 1150V. Device temperature was set at 82°C to match expected use conditions.

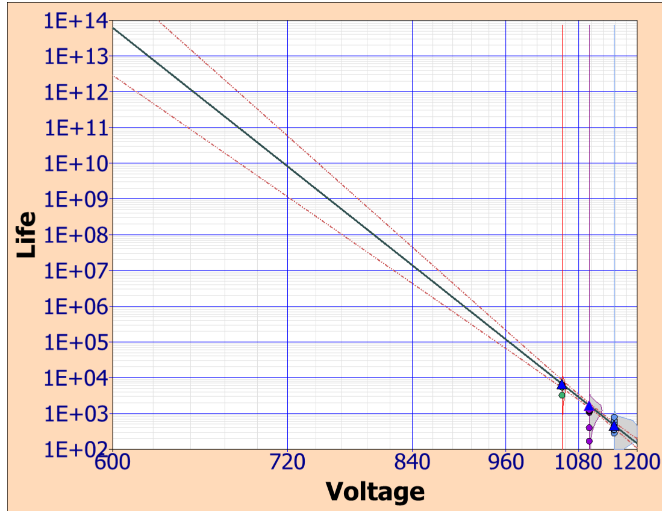


Figure 6. Log time vs. 1/V plot of HVOS testing using a linear TDDB model for illustration of data integrity (projection may not provide the device lifetime)

Figure 6 shows the failure times vs. voltage for one possible failure model: linear voltage time dependent dielectric breakdown. This particular model is used to most easily illustrate the results but does not represent the reported high field lifetime prediction. The reported prediction is based on a reciprocal voltage time-dependent dielectric breakdown model that represents the most conservative lifetime as shown in Figure 7.

Similar to the Arrhenius plot of Figure 5, the small range of failure times around the MTTF points demonstrates the quality of the test. The 95% confidence limits (dashed lines) give a strong support to the projected lifetimes reported. The slope of the line provides the acceleration factor needed to provide a physical understanding.

While the plots above are useful for understanding the reasons behind the devices failing, the use-plots of Figures 7 and 8 are more useful in understanding the process lifetime and reliability. In each plot, all devices (including multiple sample sets) tested at accelerated conditions are projected back to a use condition using the physical parameters determined from the plots above.

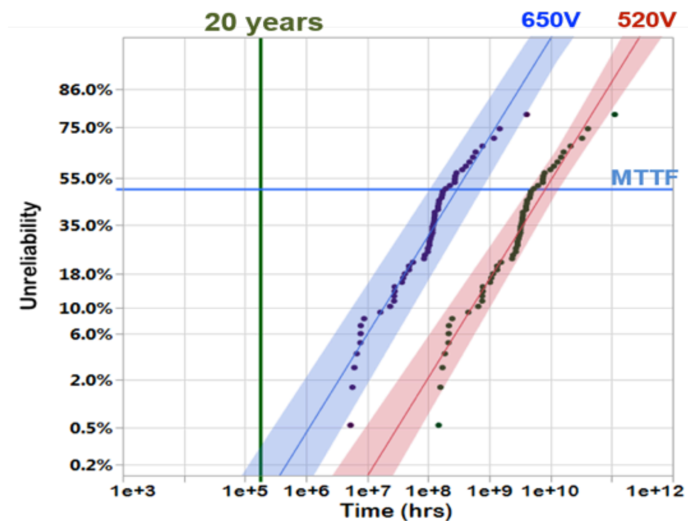


Figure 7. Use-plots based on voltage accelerated testing showing all failed devices during HVOS testing for the reciprocal field TDDB model. This is the most conservative of the five most commonly used models.

The Weibull plot combines all of the devices into a single set and allows a more detailed understanding of the variability of the process as well as predicting device lifetime.

The results in Figure 7 are from high field testing of sample sets across six lots. High field lifetime at 650V or 520V as shown can be directly taken from the plot, not only at 50% failures (>1 x 108 hours), but also at low percentages such as 10% (~1 x 10^7 hours) or 1% (~2 x 10^6 hours). The relatively steep slope of the multiple sample sets shows the small variability of the process lot to lot as well as within a wafer. The 95% confidence limits provide assurance that the projected lifetime for 1% failures is >1 x 10^6 hours. Additionally, the first failures do not form a significant tail. The lack of a tail indicates that the field related FIT rate will remain low for the lifetime of the devices.

Similar to the field related use-plot, the temperature related use-plot of Figure 8 shows median lifetime of >2 x 10^7 hours at the peak rated junction temperature of 175°C. The steep slope of the fitted line and the narrow 95% confidence limits show that the small variability of the process. Device and test time availability contributed to limited sample sets, but the robustness of the high temperature results and the 1.8 eV activation energy that matches reported values give us great confidence in the reliability of our standard products.

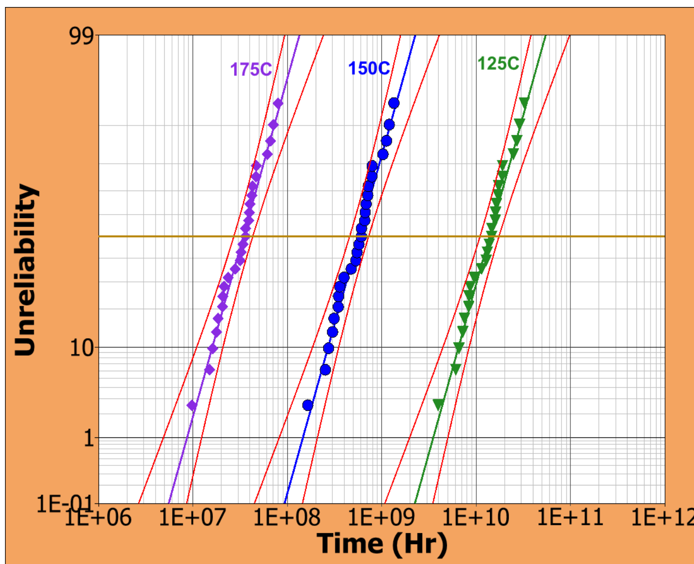


Figure 8. Use plot of all HTDC device failures at three different use-temperatures

Transphorm has the longest history and largest database of experimental test data on the complete reliability lifecycle of high-voltage GaN. We have proven that widespread adoption of GaN for power conversion applications is low-risk. Through JEDEC-style testing and HTOL, we have shown that the initial quality and robustness of our process is more than sufficient for the successful implementation into a wide variety of demanding user applications. The projected mean lifetimes for both the on-state and off-state are greater than 1 x 10^7 hours at nominal operating conditions, which exceeds the requirements of any known system. FIT analysis from HTRB testing has predicted a low failure rate of less than five parts per billion hours and is supported by the small variability seen in the highly-accelerated testing. The quality and reliability of Transphorm’s GaN power devices has been shown to be as good as or better than silicon power devices. Transphorm’s power GaN products are produced using the same high quality methods and materials as silicon power products and are validated with stress-testing beyond JEDEC standards such that the reliability of our GaN products should be indistinguishable from the reliability of silicon products.

RELIABILITY ASSURANCE

In order to ensure Transphorm's products continue to be reliable we have launched a Reliability Assurance Plan (RAP) that involves periodic sampling and reliability testing of its products. Each quarter the most "aggressive" qualified product is randomly sampled and subjected to highly-accelerated stress testing (HAST) three times in excess of JEDEC-type qualification tests.

Typical reliability assurance plan implementation:

- HTRB 3000 hours
- Power cycle: 30,000 cycles
- Temp cycle: 2000 cycles
- HAST 288 hours

CHANGE CONTROL

Transphorm is committed to continuous improvement of its products and processes. A careful, deliberate, well documented, and thorough change control process is an essential element of our continuous improvement programs.

The entire change control process is managed by the Change Control Board (CCB) which is made up of senior quality, device, and operations personnel. At inception all proposed changes are "classed" by the CCB depending on the risk/benefit of the change. Each class of change represents a certain level of qualification before the change is allowed into the production line.

Table 2. Change Control Board (CCB)

Class	Definition	Minimum requirement
1	Major change. Data sheets affected. Visible to customer. Potential change to fit, form or function.	Full JEDEC qualification. PCN required.
2	Possible change to performance. Not visible to external customer.	48 hrs. high voltage stress on 3 split lots (minimum 1 wafer per lot). All etest and physical audit/inline SPC data within 95% confidence interval of POR data to be submitted as validation data.
3	No change in performance. Not visible to external/internal customers.	3 split lots (minimum 1 wafer per lot) hard spec yield. All etest and physical audit/inline SPC data within 95% confidence interval of POR data to be submitted as validation data.
4	No impact on process or performance.	3 wafers from 2 lots (minimum 1 wafer per lot) Physical verification only. All physical audit/inline SPC data within 95% confidence interval of POR data to be submitted as validation data.
5	Initial process investigation, no changes to POR.	No minimum wafer requirement. May be short loop or full loop experiments. If changes to POR are desired based on test results, document should be revised and experiment repeated as Class 1 through 4.

If a change is considered a Class 1 change, then potentially a Process Change Notification (PCN) along with representative samples of the product, must be issued to the effected customers, at least 90 days prior to the implementation of the change. Transphorm is committed, at a minimum, to be compliant with the most current version of JEDEC STANDARD JESD46 "Customer Notification of Product/Process Changes by Semiconductor Suppliers".