Investigation of Driver Circuits for GaN HEMTs in Leaded Packages

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***Abstract*— GaN devices have superior performance over Si-based devices, but even a very small parasitic inductance makes GaN HEMT hard to drive. Many advanced leadless packages are proposed for lower parasitic inductance to fully realize advantages of GaN devices. However, leaded packages are still dominant in industrial applications because of their simplicity for PCB assembly and capability for a wide variety of heat-sinking techniques. In this paper, the performance of a basic half bridge power circuit based on GaN HEMTs with TO package (TO-220) is analyzed, and GaN device driver design is also discussed. Simulation and experimental results are provided for validation.**

Keywords—GaN HEMT; leaded package; driver; ferrite bead

I. INTRODUCTION

Currently widely used in LEDs, Gallium Nitride (GaN) is the next generation in power electronics. The GaN transistor combines low switching and conduction losses, offering reduced energy loss of more than 50 percent compared to conventional silicon-based power conversion designs. Transphorm Inc. has established the industry's first qualified 600-V GaN device platform with its TPH3006PS GaN HEMT. The TO-220-packaged device features R_{ds}(on) of 150 mΩ, Q_{rr} of 56 nC and high-frequency switching capability that enables compact lower cost systems [1].

Two types of TO-220 600-V GaN HEMTs are provided which have Source Kelvin Tab and Drain Tab, respectively. Soldering the tab directly to the PCB is a good way for eliminating the lead parasitic inductance so as to reduce ringing on gate and switching node, but it is not widely used in industry due to the issues of reflow soldering and heat dissipation limitation [2]. For the high power application, low thermal resistance heat sinks are necessary to mount on the tabs of GaN HEMTs, and PCB layout with leads connection should be studied.

II. GATE DRIVER CIRCUIT FOR GAN HEMTS

The GaN device manufactured by Transphorm, Inc. is the cascode structure which incorporates a normally-off low-voltage (LV) Si MOSFET at the input and a normally-on high-voltage (HV) GaN HEMT at the output, as shown in Fig. 1. The switch is turned on and off by controlling the low voltage MOSFET, so the gate driver circuit is same as high voltage Si MOSFET. Fig. 2 shows a half bridge circuit schematic with non-isolated half-bridge boot-strap driver. By adjusting the gate resistor, the switching speed of LV MOSFET can be controlled, but it has little impact on GaN HEMT switching speed. Slowing down the switching speed helps to reduce the oscillation on the gate and makes the circuit stable. However the switching loss will increase due to the increasing switching time.

The TO-220 package unavoidably adds inductance in the source lead [3], as shown in Fig. 3. This inductance cannot be further reduced, and so its impact must be recognized and mitigated. The normal expectation when a voltage signal develops across a source impedance is that it will subtract from

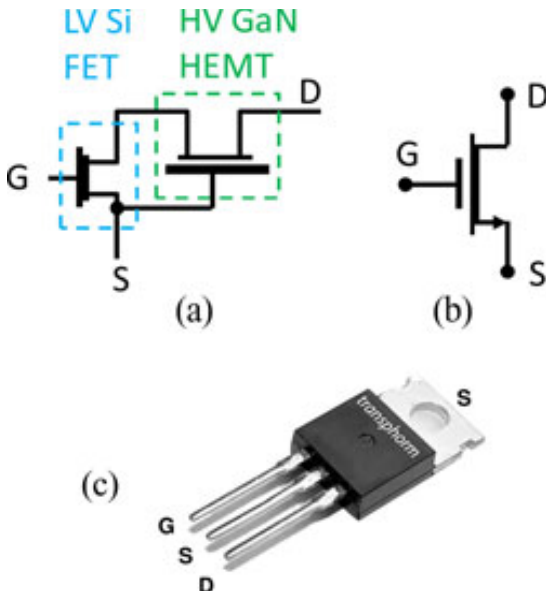


Fig. 1: GaN hybrid HEMT incorporating a LV normally-off Si FET and an HV normally-on GaN HEMT (a) to achieve a combined, normally-off device (b) in a Quiet-Tab TO-220 package (c).

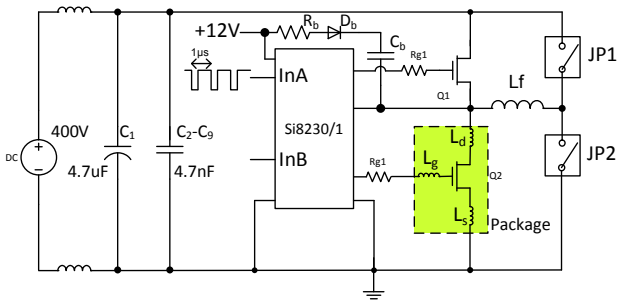


Fig. 2: Half bridge circuit schematic, JP1 is for low side device testing, JP2 is for high side testing.

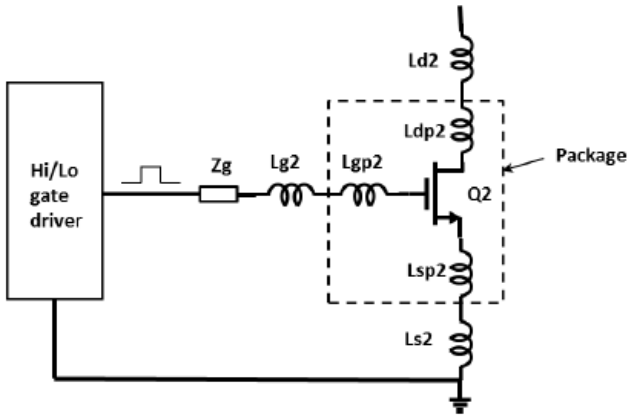


Fig. 3: input loop showing parasitic inductances internal and external to the transistor package

the gate-drive voltage and slow the turn on. Slowing the di/dt transition by reducing i_g will indeed reduce the corresponding source voltage during that part of the turn-on transient. Using a gate resistor in the place of Z_g in Fig. 3 would accomplish this. A gate resistor will not, however, provide the additional function of limiting slew rate at the switching node: $d(V_{ds})/dt$. This is because the feedback capacitance, C_{rss}, of the cascode combination is so low. Simply choosing a gate driver with a lower output current is a better way to limit i_g and di/dt. The voltage oscillation on the gate is mainly caused by the common source inductance. Since the threshold gate voltage of MOSFET is only 2.1 V, the oscillation voltage spike may make the device fault turn on. Under this consideration, negative voltage bias on the gate driver is proposed in the previous research [4], and boot strap half bridge driver circuit is not appropriate.

III. Simulation and Switching Test Results

A. Boot strap driver circuit

Using traditional boot strap driving method without negative voltage bias, the oscillation reduction on the gate signal is necessary. Adding a gate resistor and RC snubber to damp the ringing is a good practice in the application. In order for fast turning off the device, a reversed diode paralleled with

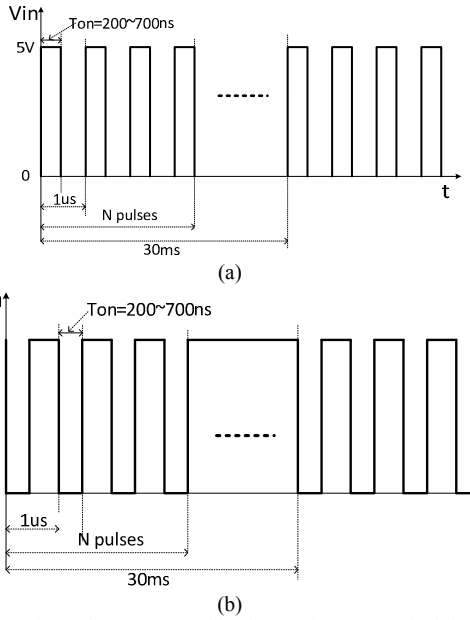


Fig. 4: Driver input signals for multi-pulse testing. (a) High side switching test when JP2 shorted; (b) Low side switching test when JP1 shorted.

R_g is applied, while due to the junction capacitance of the diode, it has less effect to turn off the GaN device fast. It is also found that a small SMD ferrite bead effectively opposes transient high di/dt current and inhibits coupling of the signal, although the voltage waveform on the gate pin is not obviously damped.

Due to the very high di/dt rating, Si8230/1 driver from Silicon Labs Inc. is selected as it consists of a half bridge MOSFETs driver and digital isolator, which provides best-in-class noise immunity due to its less than 2 pF coupling capacitance [5]. The IC can be configured as non-isolated boot strap driver with up to 1.5 kV driver to driver differential voltage, and also as an isolated driver with up to 5 kV isolation rating.

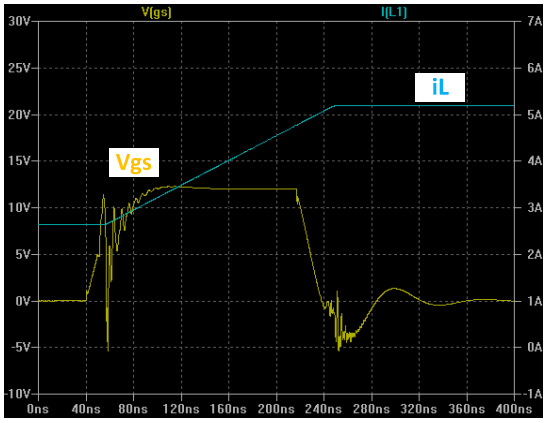
As shown in Fig. 2, for the half bridge circuit testing, the DC bus voltage is 400 V, several 4.7 nF X7R ceramic capacitors are placed between the drain of high side device and source of low side device as decoupling capacitors. 60 μH small inductor is connected to the Ground for high side device hard switching testing, and it also can be connected to the DC positive rail for low side device hard switching testing. Si8231 single input driver is selected for obtaining complementary output driving signals with 100 ns dead time. Multi-pulse driving waveforms from signal generator are shown in Fig. 4. N pulses every 30 ms interval are generated, and the pulse period is 1 μs. By adjusting pulse width and number of pulses, the switching current can be controlled. A 300 Ω at 100 MHz SMD ferrite bead from Bourns Inc. is chosen as Z_g. The same circuit model is set up in the LTspice for simulation verification.

B. *Simulation and experimental results using ferrite beads*

Fig. 5 shows the simulated and measured V_{gs} waveforms during turn-on time; voltage oscillation can be observed in both figures. This oscillation is caused by the source inductance and couples to the gate pin. The real internal gate voltage is clean, indicating that the device didn't turn on or off incorrectly, as shown in Fig. 6. Fig. 7 shows the high side device can hard switch at 41.6 A with V_{ds} undershoot no more than -100 V; Fig. 8 shows the low side device can hard switch at 27 A with V_{ds} spikes no more than 600 V. The device can switch in such high current rating that the circuit is robust to survive at high current stress transient conditions. Due to the undershoot voltage applying on the boot strap circuit during charging the boot strap capacitor, a 10 ~ 15 Ω, 0.5 W resistor R_b is connected to the circuit to limit the inrush current and an ultrafast 600 V 1 A diode is chosen as D_b.

C. *Effect of ferrite beads*

Different value of ferrite beads are applied and compared. Low side hard switching waveforms are shown in Fig. 9. It can be seen that, large ferrite bead helps to reduce the voltage spikes, but it brings longer turn on / off time delay. As shown in Fig. 10, in the condition of 15 A switching current, the turn



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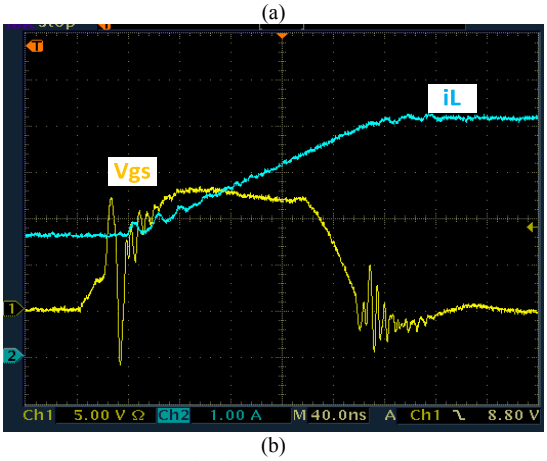
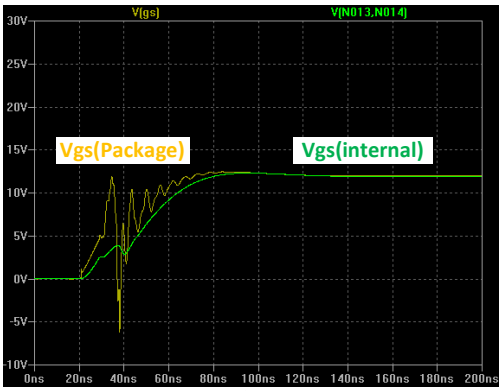


(b)

Fig. 5: Comparison of simulated and measured Vgs waveforms and output current. (a) Simulated V_{gs} (on package pins); (b) Actual Vgs in the experiment (on package pins).



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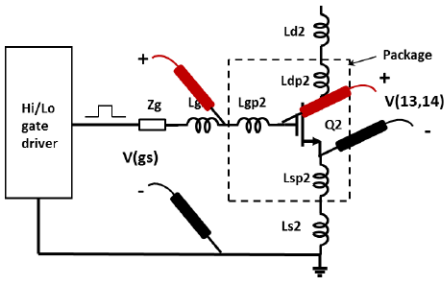

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Fig. 6: Simulation showing the measured V_{gs} and internal V_{gs}. (a) Simulation waveforms; (b) Voltage probing point.

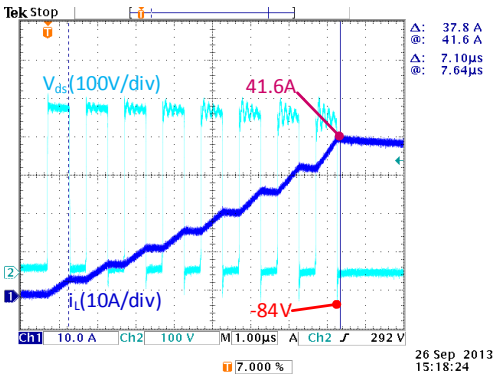


Fig. 7: High side switch multi-pulses test.

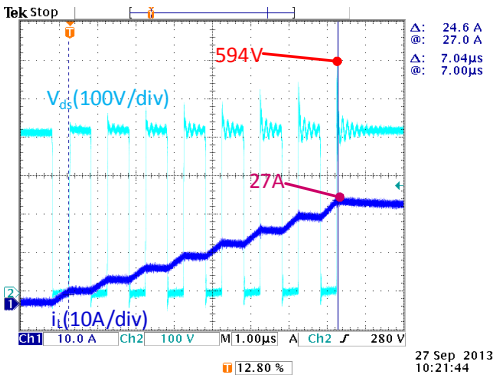
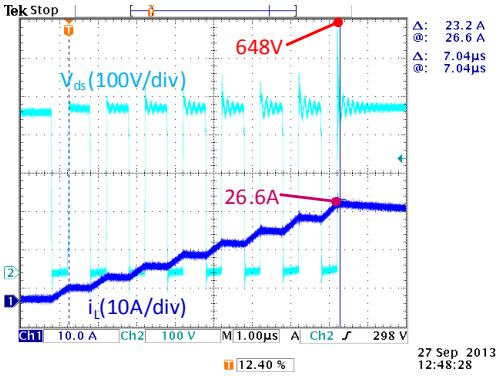


Fig. 8: Low side switch multi-pulses test.



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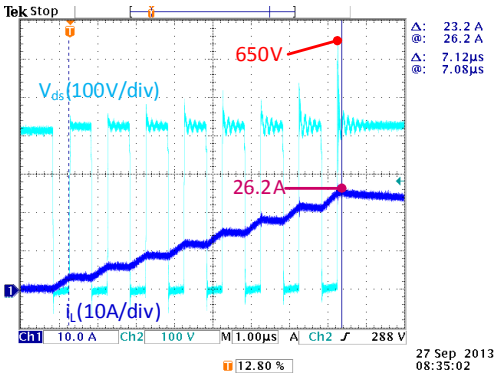

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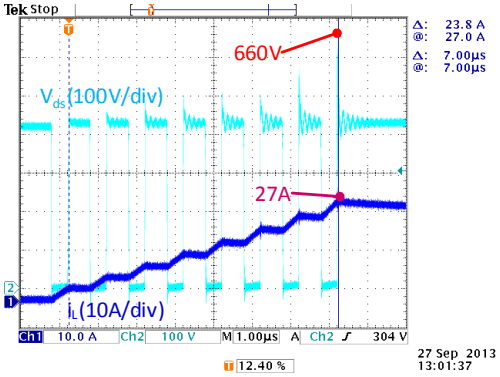

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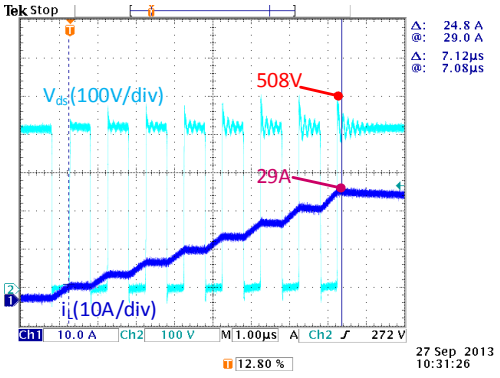
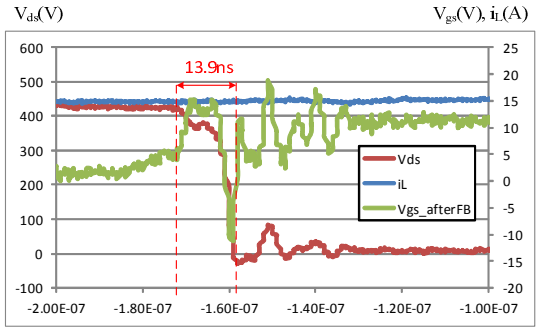


(d)

Fig. 9: Low side switching waveforms with different ferrite beads. (a) TDK 80 Ω MMZ2012D800B; (b) TDK 120 Ω MMZ2012D121B; (c) Wurth 120 Ω 74279202; (d) Taiyo 430 Ω BK2125HS431-T.



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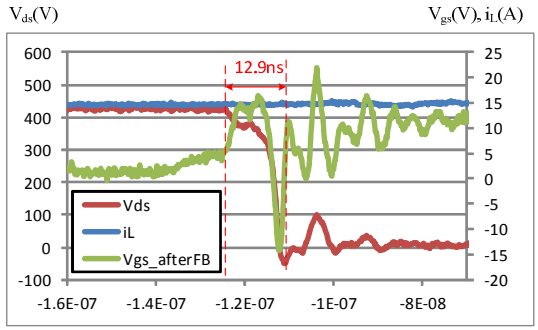

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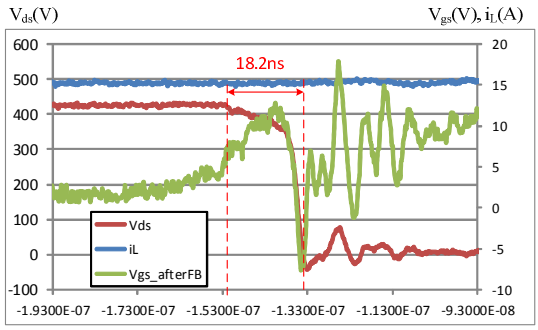

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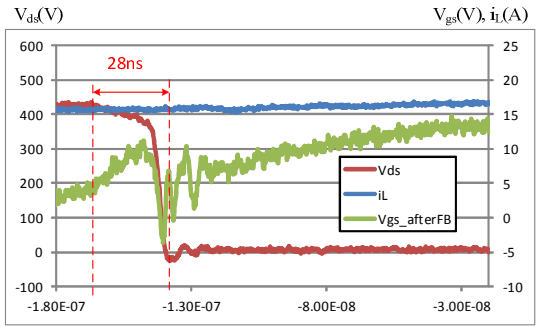
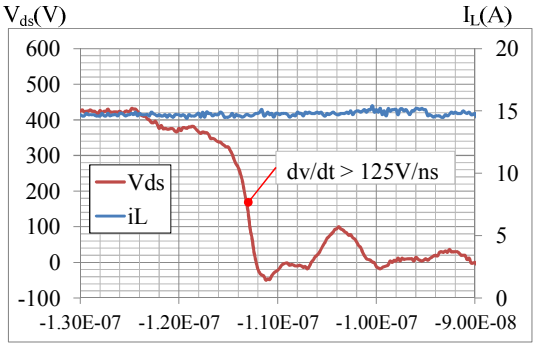


(d)

Fig. 10: Turn-on crossover time with different ferrite beads. (a) TDK 80 Ω MMZ2012D800B; (b) TDK 120 Ω MMZ2012D121B; (c) Bourns 300 Ω MU2029-301Y; (d) Taiyo 430 Ω BK2125HS431-T.

on crossover time of V_{ds} and I_d increases from 12 to 28 ns with the ferrite beads' value increasing. Compared to Z_g = 0 at 10A in [6], there is only additional 2 ns longer for 120 Ω ferrite bead even at 15 A. In the high switching frequency application, 120 Ω or less value of ferrite bead is proposed. Fig. 11 shows the ferrite bead solution does not reduce the switching speed.



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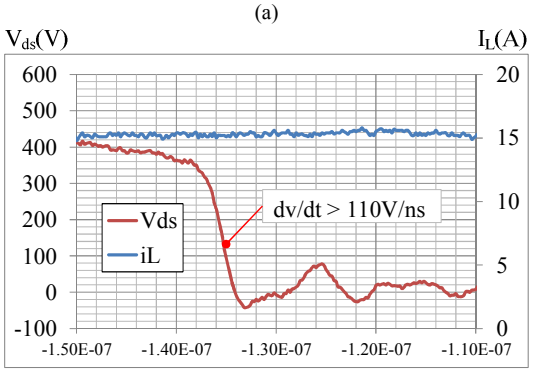


(b)

Fig. 11: Turn on dv/dt at 15 A with different ferrite beads. (a) TDK 120 Ω ferrite bead; (b) Bourns 300 Ω ferrite bead.

Even with 300 Ω ferrite beads, the dv/dt is still over 110 V/ns, indicating the efficiency will not be impacted.

D. Off-state margin and negative gate voltage

The previous analysis shows the internal gate voltage of the actively switched transistor. Also of interest is the behavior of the opposite transistor which should be held off during the transient. Fig. 12 shows a half bridge where the high-side transistor is switched and the low-side transistor carries the free-wheeling current. When Q_H turns on, the high dv/dt at the switching node (S) will induce current I_{GD} which charges C_{GD} of Q_L. Some of this current will flow in C_{GS}, raising the gate voltage with a high enough ratio of C_{GD}/C_{GS}, V_{gs} could potentially increase enough to turn on the low-side switch. However, in the cascode device this ratio is extremely low. For the TPH3006, for example, C_{GD} is 4.5 pF while C_{GS} is 720 pF at V_{gs} = 0 and over 2000 pF at the onset of turn-on.

A more valid concern than capacitive coupling through C_{GD} of the cascode pair is coupling through C_{GD_Si} of the low-voltage silicon FET. The drain-source voltage of the silicon FET, V_{ds_Si} in Fig. 12, only rises to $-V_{th}$ of the GaN HEMT, but will do so with high dv/dt. The ratio of C_{GD_Si}/C_{GS} in this case is significant. Fig. 13 compares external gate waveforms for measured and simulated cases. The simulation also includes the internal V_{gs} of the silicon FET. It is seen that V_{gs} does rise quickly toward the threshold voltage when V_{ds_Si} changes. However, because the rise in V_{ds_Si} corresponds to turn-off of

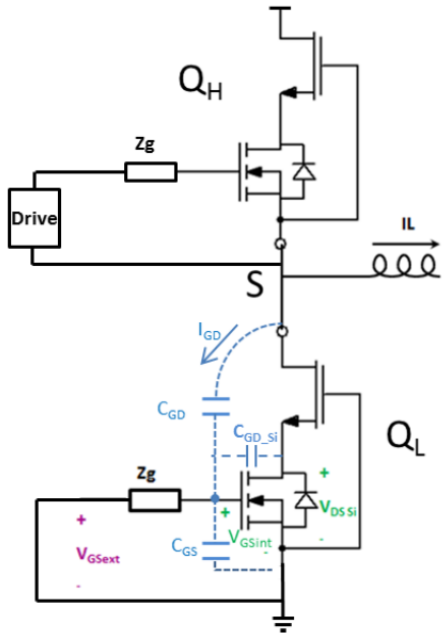
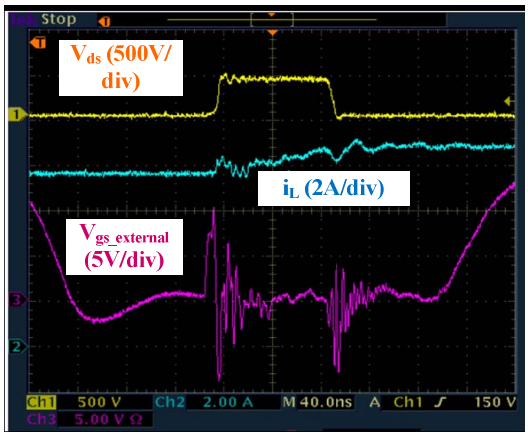


Fig. 12: Capacitances of the off-state transistor: Q_H is actively switched, Q_L is off.



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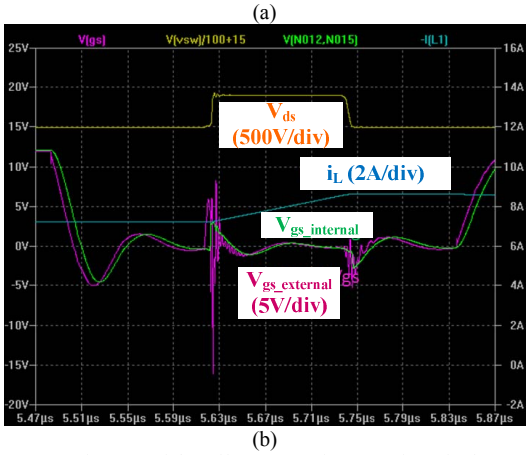

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Fig. 13: Capacitances of the off-state transistor: Q_H is actively switched, Q_L is off.switched, Q_L is off.

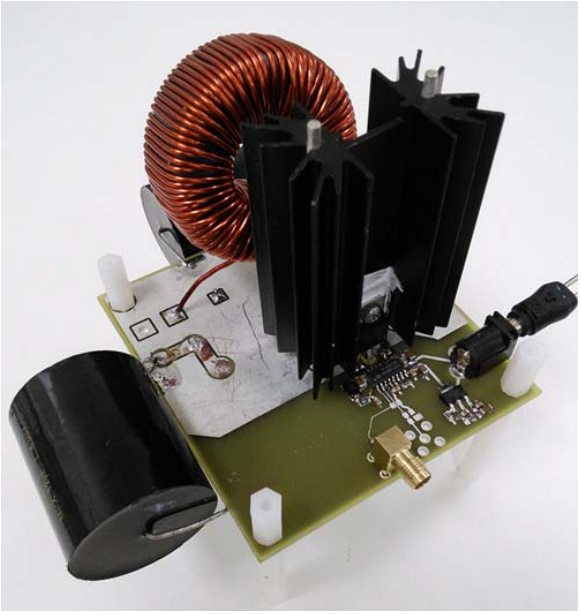
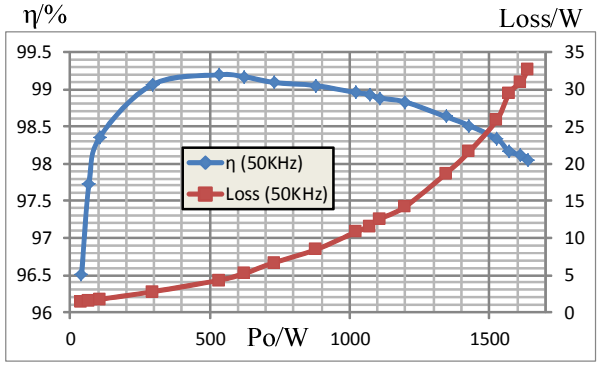


Fig. 14: Photo of half bridge converter with TPH3006 GaN HEMTs

the GaN HEMT, any drain current induced in the silicon FET due to the rise in V_{gs} must first discharge the GaN gate before external current flows.

IV. Efficiency Test

As shown in Fig. 14, a half bridge boost converter operating in synchronized mode was designed for 200 V input and 400 V output. 15 µF/630 V and 9.4 µF/630 V film capacitors are applied in the input and DC bus output. A 1 mH/76 mΩ boost inductor is employed, which is made up of two layers of AWG18 windings and a MPP core C055439A2 from Magnetics Inc. The back-to-back TPH3006PS GaN HEMTs as high side and low side devices are mounted on a standard heat sink with 2.6 °C/W at natural convection condition. Both tabs of GaN HEMTs are insulated from the heat sink as it can be connected to the power ground or the earth. The capacitance between the Tab of low side HEMT and surface of heat sink will not bring switching loss as the low side has the quiet source tab. If high side device is TPH3006PS, thick ceramic thermal pad or low permittivity insulator should be used to reduce the capacitance between TO-220 tab and heat sink so as to eliminate the extra switching loss. A fan placed towards to the heat sink providing 80 CFM air flow can keep the maximum temperature of heat sink below 95 °C at 1650 W output power. It is impossible to achieve such high output power using surface mount package device such as PQFN device without using aggressive active cooling method. In Fig. 15, it can be seen that the efficiency is over 99% over the wide load range for 50 kHz switching frequency. And the peak efficiency is 99.2% at 530 W output power, while for 100 kHz switching frequency it is still over 98.9% at 680 W output power.



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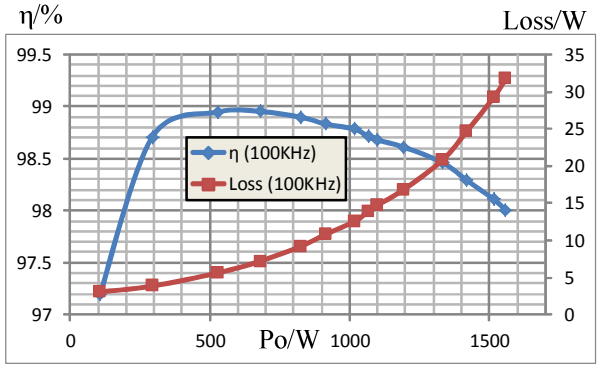

(b)

Fig. 15: Efficiency and power loss vs. output power at switching frequency: (a) 50 kHz; (b) 100 kHz

V. Conclusion and Future Work

In this paper, the driver circuit of half bridge for leaded package GaN HEMTs is analyzed, and the effect of different ferrite beads is discussed in detail. A simple and robust boot strap half bridge driver circuit is proposed for high power half bridge converter applications. The simulation and experimental results shows the GaN HEMTs can safely operate at very high current rating in hard switching condition, while the switching speed does not slow down thus helping maintain the high efficiency.

In the future work, in order to reduce the high voltage spike due to the PCB layout limitation in application, RC or RCD snubber circuit will be explored although it will bring additional 0.1 ~ 0.2% efficiency drop. Isolated power supply circuit for providing negative bias voltage and insulation will also be analyzed, which is also very popular in high power applications. However, due to lack of high speed common mode transient immunity (CMTI) ICs and power supplies, high speed switching noise may result in severe interference between power circuit and signal circuit.

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