WHITE PAPER

Reliability Lifecycle of GaN Power Devices

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March 2017

transphorm

Highest Performance, Highest Reliability GaN

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Introduction

From its inception Transphorm has performed comprehensive reliability testing of its products and has achieved industry firsts in qualifying 600V and 650V GaN products for the marketplace. Transphorm has continued to expand testing to determine quality, FIT levels and long term reliability of its products.

Transphorm utilizes standard JEDEC qualification testing prior to commercializing its GaN power devices to ensure that the quality of GaN devices will meet customer expectations for reliability. The JEDEC tests were originally developed on silicon technology and it is appropriate to examine the assumptions that underlie the tests and determine the level of protection that these tests offer for GaN products. Transphorm's testing has also gone beyond the minimum requirements of JEDEC testing by running tests on a much larger number of devices than the minimum required.

Beyond initial quality, we have used accelerated testing to predict how long the devices will last. High temperature testing has been used to predict device lifetimes due to temperature related degradation as the devices are passing current at low voltages. The high voltage rating of the parts is related to the blocking portion of operation, so high field testing has been used to evaluate this portion where there is no current and the voltages are high. Additionally, the transition between the two operating conditions has been tested by operating the devices for extended periods of time at maximum operating conditions.

Bathtub curve and reliability

The bathtub curve is typically used to represent the three phases in a product's reliability history. An "Infant Mortality Phase" is characterized by relatively large numbers of early failures with a decreasing frequency. The flat part of the bathtub curve represents a relatively small numbers of failures at a constant frequency, and the wear out period starts with a relatively small numbers of failures, whose frequency increases over time.

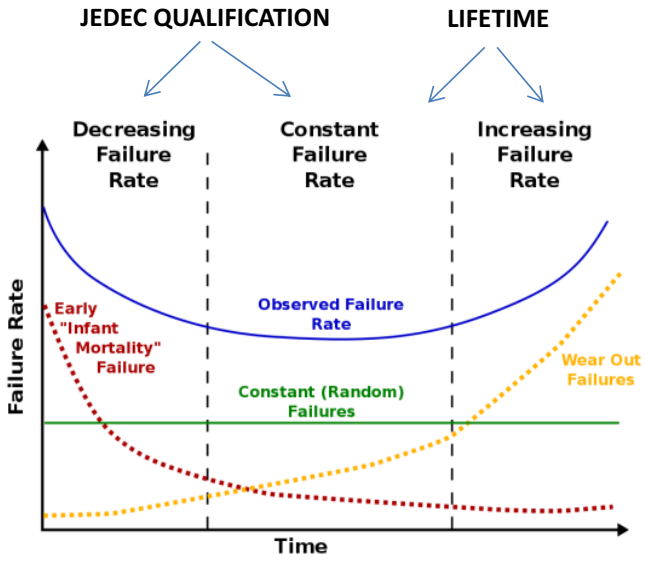


Figure 1. Reliability lifecycle illustrated using a "bathtub curve"

JEDEC qualification

JEDEC testing typically utilizes relatively large numbers of devices, and applies a fairly modest level of stress to those devices. The tests are designed to give a lot of information about infant mortality, and a limited amount of information about the constant failure rate portion of the bathtub curve and virtually nothing about the wear out failure portion. Table 1 illustrates the tests that comprise Transphorm's typical JEDEC qualification test set.

Table 1. JEDEC qualification test results for Transphorm's products

Test	Symbol	Conditions	Sample	Pass Criteria
High Temperature Reverse Bias	HTRB	TJ=150°C VDS = 480V 1000 Hrs	3 lots 77 parts per lot 231 total parts	0 Fails
Highly Accelerated Temp and Humidity Test	HAST	130°C 85% RH 33.3 PSI Bias = 100V 96 Hrs	3 lots 77 parts per lot 231 total parts	0 Fails
Temperature Cycle	TC	-55°C / 150°C 2 Cycles / HR 1000 Cycles	3 lots 77 parts per lot 231 total parts	0 Fails
Power Cycle	PC	25°C / 150°C ΔT = 100°C 7500 Cycles	3 lots 77 parts per lot 231 total parts	0 Fails
High Temperature Storage Life	HTSL	150°C 1000 Hrs	3 lots 77 parts per lot 231 total parts	0 Fails

In addition to these electrical tests, there are the standard mechanical tests for die attach and bond wire strength typical for any semiconductor products. By passing this suite of tests we have some assurance that our products are free from any of the typical defects that can have a negative impact on short-to-medium term reliability.

Given that we understand that JEDEC qualification is focused on the first two phases of the bathtub curve (we address the wear out phase later in this paper) we can examine Transphorm's standard and extended qualification results.

Defect density and sample size

The more parts that we sample in any qualification test, the more likely we are to sample a part that fails. The industry standard test, which has been influenced very heavily by automotive quality requirements, is to test three lots, with 77 parts in each lot, and passing the test with zero failed parts (3 x 0/77), out of a total sample size of 231. This testing scheme satisfies the <3% Lot Tolerance Percent Defective (LTPD) quality level as per JESD47, and all Transphorm products must meet this standard before being released to production.

How sensitive is the standard test? One way to look at the sensitivity of any sampled test is to plot its operating characteristic (OC) curve (Figure 2), which show the probability of passing the test (Pa) vs the actual number of defective parts (Do).

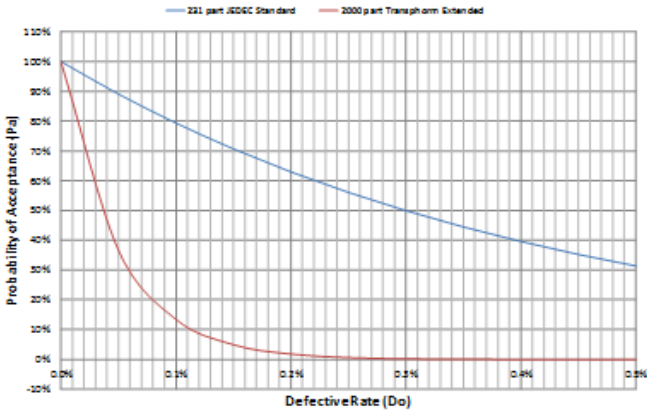


Figure 2. Operating characteristics curve showing the low defect rate predicted by the 2000 part test with no failures

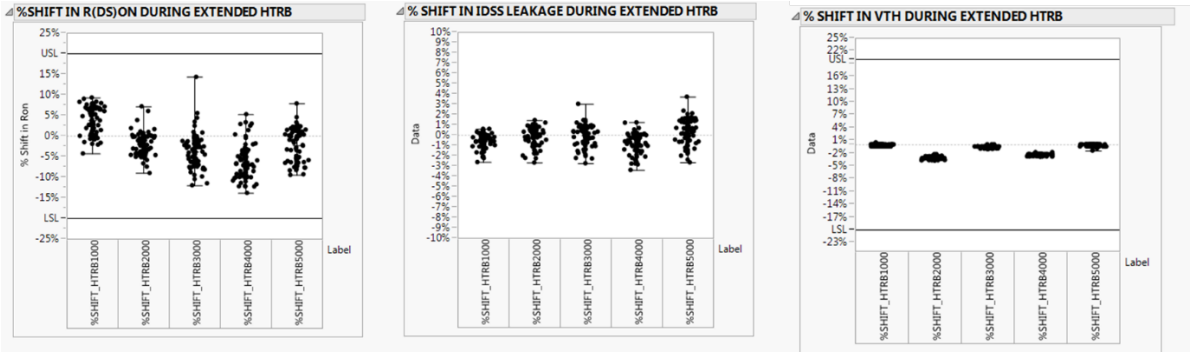
The first curve (blue) demonstrates that in order to have a better than 95% chance of passing the standard JEDEC test, defect levels need to be below 0.022% or the probability of passing the test drops rapidly.

While this standard has served the semiconductor industry well for gating the entry of products into the field, a new

product has a reasonable chance of passing at an unacceptably high defective rate. It has become common practice to run larger samples over an extended period of time to gain a better understanding of defective levels and generate better confidence that the defective levels are low, as shown by the red curve.

Transphorm has completed HTRB testing on over 2000 parts for 1000 hours without failure. By testing many lots over an extended period of time Transphorm tests the intrinsic capability of its device, and also tests the stability of the production operation over time. The 2000 parts were samples in batches of ~50 parts in each lot during the course of 12 months of production time. To have a 95% probability of passing that test the defect levels needs to be below .003%, as shown by the red curve. This represents more than an order of magnitude improvement in quality over the standard JEDEC qualification scheme. **Additional extended reliability tests have included running 80 parts for 5000 hours of HTRB, and 480 parts at 650V HTRB, all without failure.**

5000 Hour HTRB Data Showing Parametric Shift Data That Easily Passes Q101 Criteria



Transphorm is committed to perpetual reliability testing of its products and is continuing to test. Transphorm's extended samples are large enough to detect very low levels of defects, and continuous testing and improvement will help ensure high quality. However, JEDEC qualification does not directly predict field failure rates.

High temperature switching operation test

During normal operation, the devices are exposed to many of the JEDEC test conditions simultaneously. High temperature operating life test (HTOL) mimics hard switching conditions in applications and provides a window into possible interactions affecting reliability. We ran the test on standard parts operating as the main switch in a boost converter. The devices were run at 175°C junction temperature, which is higher than the 150°C reported in the data sheet. The higher temperature provides a minor acceleration of the test, but higher temperatures result in the degradation of external components thereby limiting the maximum junction temperature to 175°C. Figure 3 shows conversion loss of the devices over the life of the HTOL. Degradation of the solder contacts and external components in the circuit are the reasons for the increase in conversion loss after 2000 hrs; the devices showed no significant change in performance when measured after the HTOL. While this test does not predict lifetime, the GaN devices are robust for extended times at the maximum rated temperature in actual operating conditions.

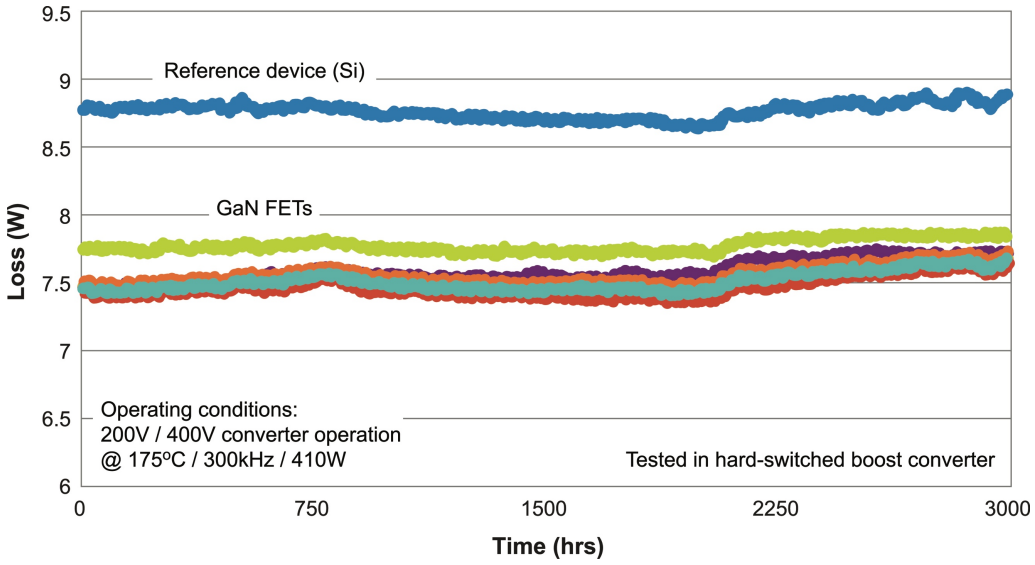


Figure 3. Loss plot for HTOL of seven 600-V-rated GaN-on-Si FETs and a reference device to 3000 hours at Tj=175°C; each device operated in a boost converter at 300kHz with a boost ratio 200V:400V, 410W output power

Wear out testing

The predicted lifetime or point that the parts will begin to fail at an increasing rate due to aging is the last region shown in Figure 1. Lifetime projections which depend on understanding and modeling the wear out process are based upon accelerated testing to failure. The operating conditions of a power switch allow for separation of the major stress factors. In the off-state, the device is blocking a large voltage across the switch with no current flowing in both normal operation and in accelerated voltage testing, allowing for high field testing and lifetime projections without the complications of current and/or temperature extremes. In the on-state, the device is conducting medium levels of current with a small voltage across it that is similar at both nominal and elevated temperature operation needed for lifetime predictions. The combined understanding from on-state and off-state testing provides confidence that the wear out predictions are accurate. The use of proven materials and processes within standard specifications has made high current testing a low priority.

We have used temperature accelerated testing to project on-state lifetimes to be > $1x10^8$ hours. Temperature acceleration is the most common method of projecting device lifetime in III-V semiconductors. The tested devices were standard parts from production runs. The parts were operated in the on-state with a constant current. This maintained constant power dissipation and therefore constant device temperature. Three set of devices were run at separate high temperatures to provide the physical understanding and lifetime projections based on temperature related degradation.

Figure 4 shows failure times plotted on a graph of log time versus 1/temperature in Kelvin (Arrhenius plot). Each set of devices is represented by a mean time to failure (MTTF) point (triangle) or the point at which 50% of the devices are failed. A line is fitted to the MTTF points. The slope of the line provides the physical understanding of the degradation mechanism, thru the activation energy. In our case Ea is 1.84eV which is in good agreement with the values reported in the literature. The line also predicts the lifetime at use temperatures such as 423°K (150°C), which is >$1x10^8$ hours.

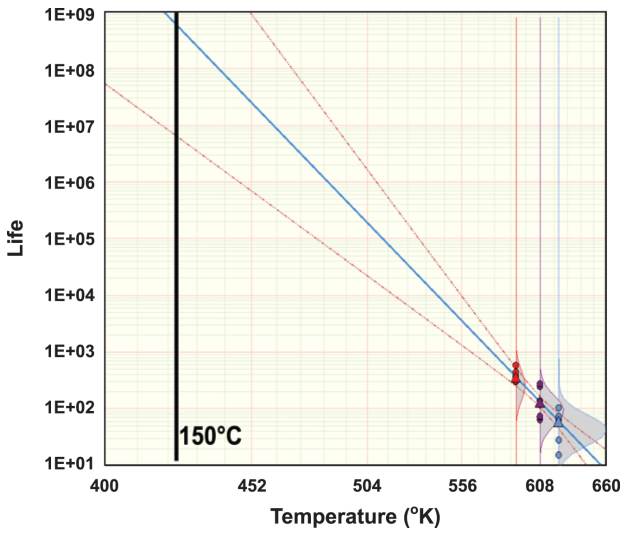


Figure 4. Arrhenius plot showing MTTFs for the 3 temperatures (in °K) and lifetime extrapolation including 90% confidence limits

The statistical validity is demonstrated both by the range of the failure points and by the 90% confidence limits shown by the dashed lines. The small range of values around the MTTF point (especially for such relatively large devices) gives us confidence that the expected failure mode is being represented. The lower limit of that range is still > $1x10^6$ hours or > 100 years at 150°.

We have shown the first report of GaN high field related lifetime of > $1x10^8$ hours at 600V. The high voltages represent a significant reliability concern but device design has limited the electric field strength to levels similar to the RF GaN devices that have been reported more extensively. Standard 600V production parts (GaN HEMTs cascoded with Si FETs) were used for the high field lifetime testing. Three sets of devices were biased in the off-state at high drain voltages of 1050V, 1100V and 1150V. Device temperature was set at 82°C to match expected use conditions.

Figure 5 shows graph of the failure times versus voltage for one possible failure model: linear voltage time dependent dielectric breakdown. This particular model is used to most easily illustrate the results, but does not represent the reported high field lifetime prediction. The reported prediction is based on a reciprocal voltage time dependent dielectric breakdown model that represents the most conservative lifetime as shown in Figure 6. Similar to the Arrhenius plot of Figure 4, the small range of failure times around the MTTF points demonstrates the quality of the test. The 95% confidence limits (dashed lines) give a strong support to the projected lifetimes reported. The slope of the line provides the acceleration factor needed to provide a physical understanding.

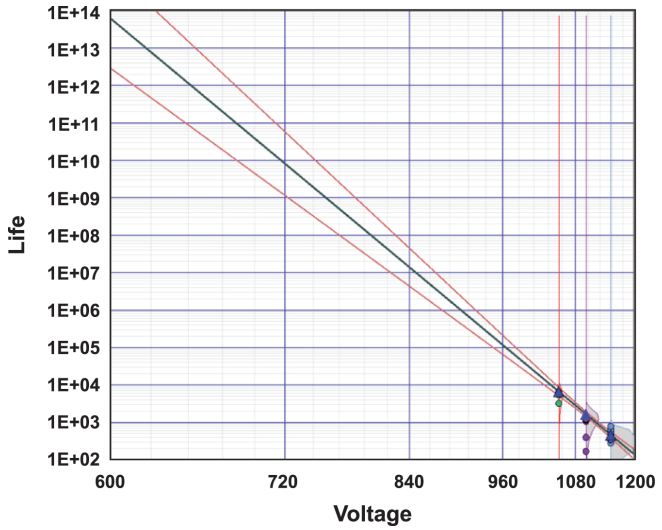


Figure 5. Log time versus 1/V plot of HVOS testing using a linear TDDB model for illustration of data integrity (projection may not provide the device lifetime)

While the plots above are useful for understanding the reasons behind the devices failing, the use plots of Figures 6 and 7 are more useful in understanding the process lifetime and reliability. In each plot, all devices (including multiple sample sets) tested at accelerated conditions are projected back to a use condition using the physical parameters determined from the plots above. The Weibull plot combines all of the devices into a single set and allows a more detailed understanding of the variability of the process as well as predicting device lifetime.

The results in Figure 6 are from high field testing of sample sets across 3 lots. High field lifetime at 650V (or 520V as shown) can be directly taken from the plot, not only at 50% failures (> $1x10^8$ hours), but also at low percentages such as 10% (~$1x10^8$ hours) or 1% (~$1x10^7$ hours). The relatively steep slope of the multiple sample sets shows the

small variability of the process lot to lot as well as within a wafer. The 95% confidence limits provide assurance that the projected lifetime for 1% failures is > $1x10^6$ hours. Additionally, the first failures do not form a significant tail. The lack of a tail indicates that the field related FIT rate will remain low for the lifetime of the devices.

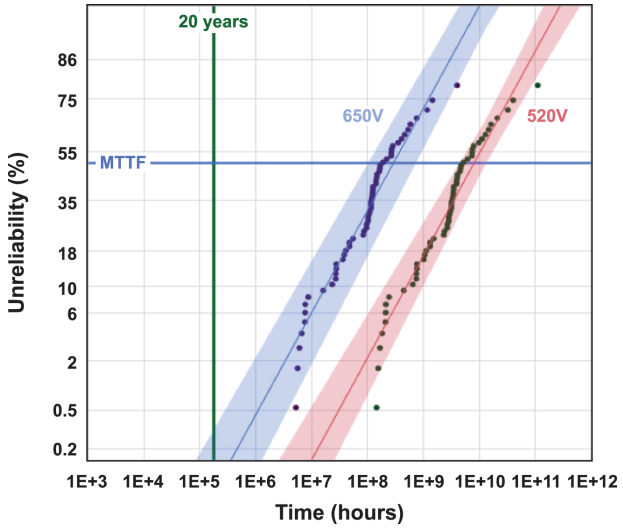


Figure 6. Use plots based on voltage accelerated testing showing all failed devices during HVOS testing for the reciprocal field TDDB model. This is the most conservative of the five most commonly used models

Similar to the field related use plot, the temperature related use plot of Figure 7 shows median lifetime of > $2x10^7$ hours at the peak rated junction temperature of 175°C. The steep slope of the fitted line and the narrow 95% confidence limits show that the small variability of the process. Device and test time availability contributed to limited sample sets, but the robustness of the high temperature results and the 1.8 eV activation energy that matches reported values give us great confidence in the reliability of our standard products.

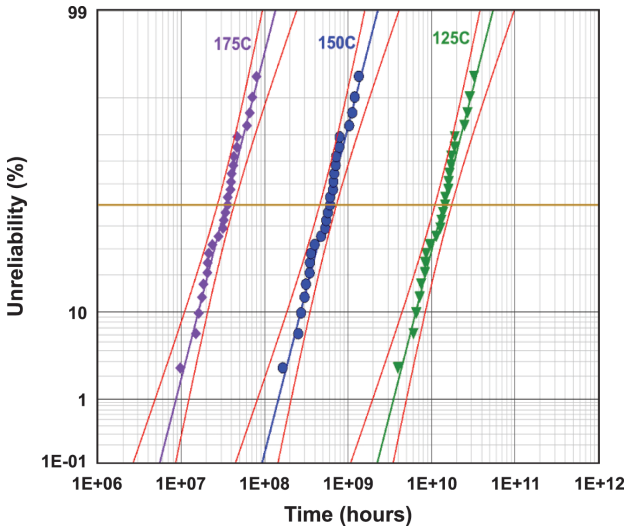


Figure 7. Use plot of all HTDC device failures at 3 different use temperatures

Conclusion

We have experimentally investigated the complete reliability lifecycle to address the perceived reliability risk that has been a major impediment to the widespread adoption of GaN. Through JEDEC-style testing and HTOL, we have shown that the initial quality and robustness of our process is sufficient for insertion in user applications. The projected mean lifetimes for both the on-state and off-state are greater than $1x10^7$hrs at nominal operating conditions, which exceeds known requirements. The quality and reliability of Transphorm's GaN power devices has been shown to be excellent. At the very least, as Transphorm's GaN products are produced using the same methods and materials as silicon products, the reliability of GaN products should be indistinguishable from the reliability of silicon products. We have validated this important hypothesis.

Acknowledgements

We would like to recognize the efforts and support of the following people central to the information in this report: YiFeng Wu, Peter Smith, Rakesh Lal, Ken Shono, Heber Clement, Sung Yea, Jim McKay, Jeffery Haller, Jose Guerrero, Donna Chandler, YuLu Huang, Bill Cruse, Yuxi Huang, Michael Diep, YuKuan Huang and Luis Martinez.