Preventing GaN Device VHF Oscillation

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Highest Performance, Highest Reliability GaN

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Parasitic oscillation

- Parasitic oscillation can occur in any switching circuit with fast-changing voltage and current that stimulate a parasitic LC network
- The oscillation becomes sustained when positive feedback with gain is present
  - The feedback could be through parasitic capacitance, parasitic inductance, shared or coupling inductance, etc.
  - Together with the device gain in the linear region, creates an oscillator
- Preventing oscillation in fast-switching GaN devices is more challenging than in silicon due to
  - Faster dv/dt and di/dt
  - Higher transconductance
- Violent sustained VHF oscillation (50-200MHz) will cause destruction

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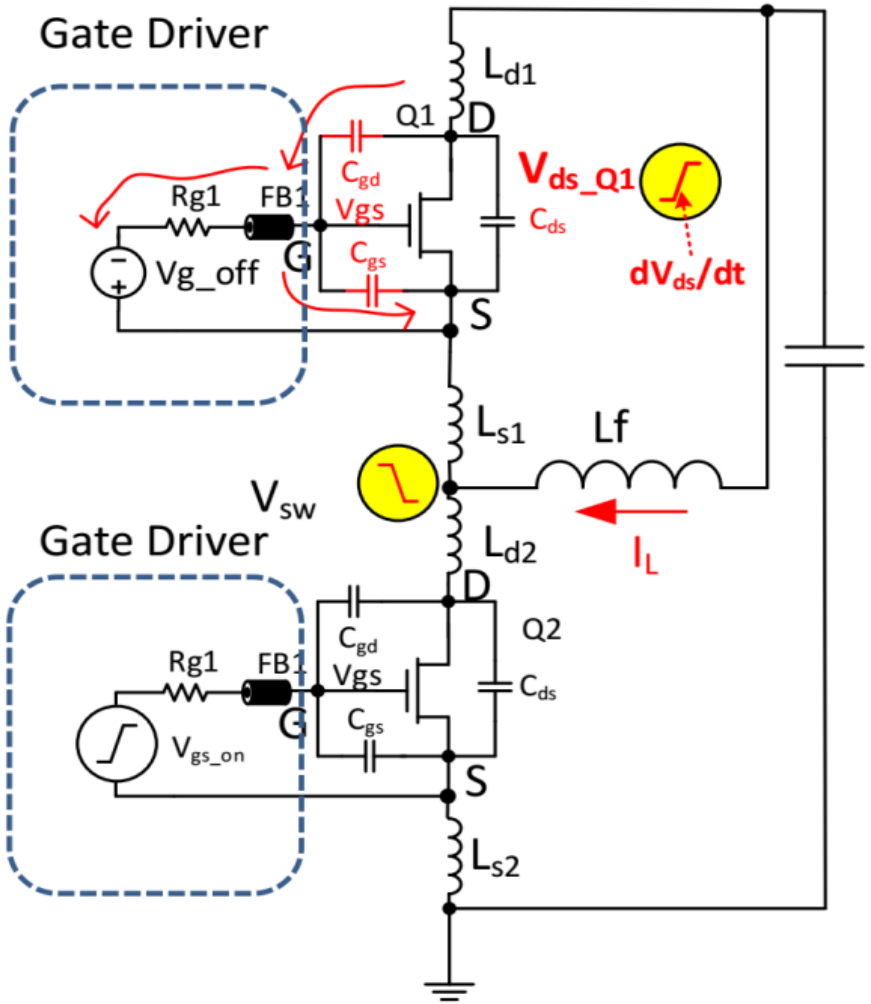
Sustained oscillation

- In a half-bridge circuit with high speed devices on both the high and low side, there are three steps that yield sustained oscillation on the high-side device during low-side device turn-on, and vice versa

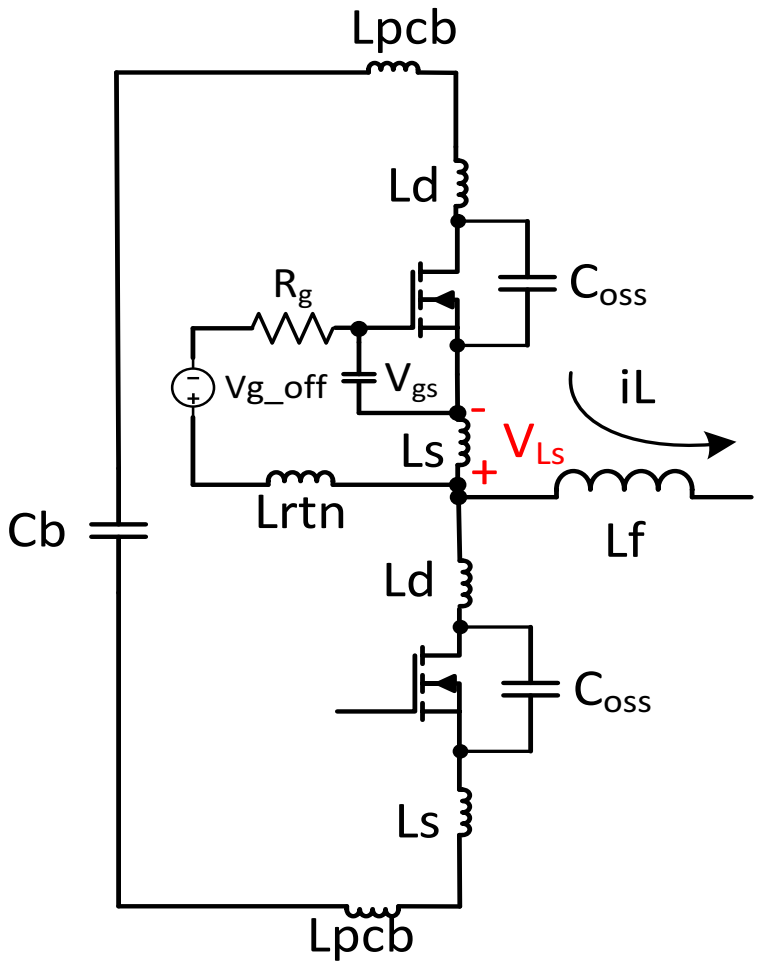
Note: Sustained oscillation can occur even in a single-ended circuit, with very fast switching, e.g. a boost converter using a FET+diode; the analysis is similar to a half-bridge

Step 1: V_{GS} change due to high dv/dt



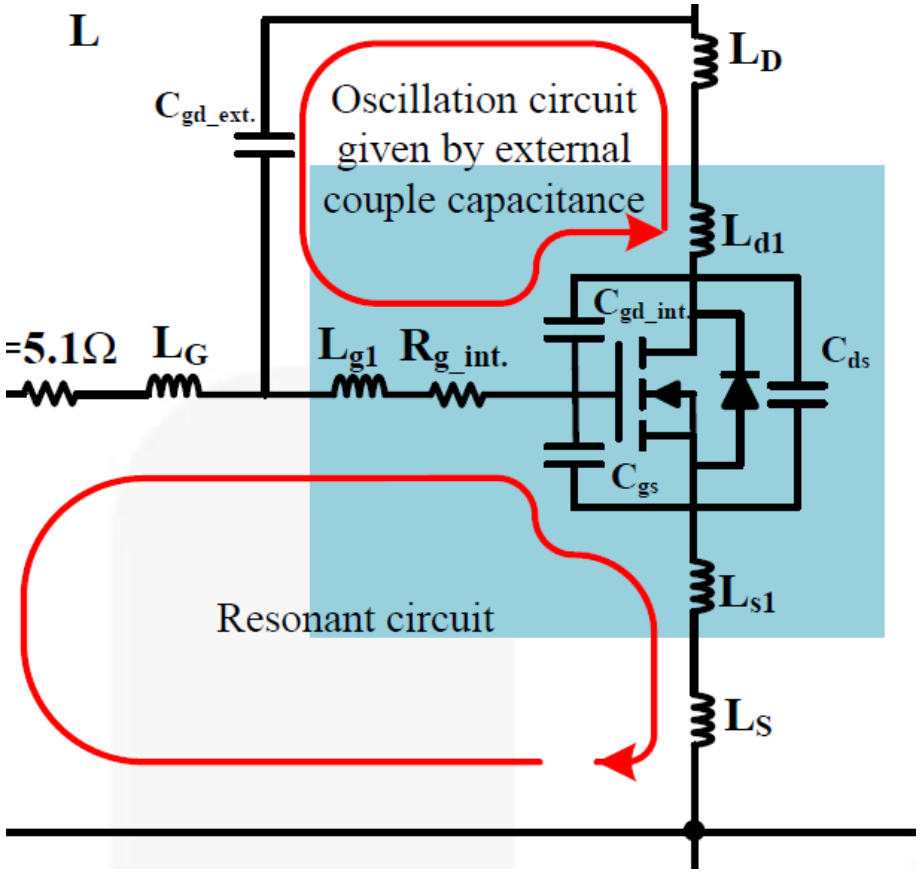
- During low-side turn-on, the high-side FET is subjected to a large positive dv/dt, which couples through C_{GD} to increase V_{GS}, ("Miller effect") reducing its off-voltage margin against gate threshold V_{TH}
- To counter this, Transphorm devices are designed with a low ratio of C_{GD} to C_{GS} to minimize the Miller effect

Step 2: V_{GS} change due to high di/dt



- During low-side turn on, the high-side FET sees a decreasing current with a large negative di/dt, which multiplied by stray inductance L_S in the PCB layout, produces a voltage V_{LS} , and also reduces the off-voltage margin
- It is necessary to have a tight layout and minimize the stray inductance

Step 3: Amplification due to transconductance

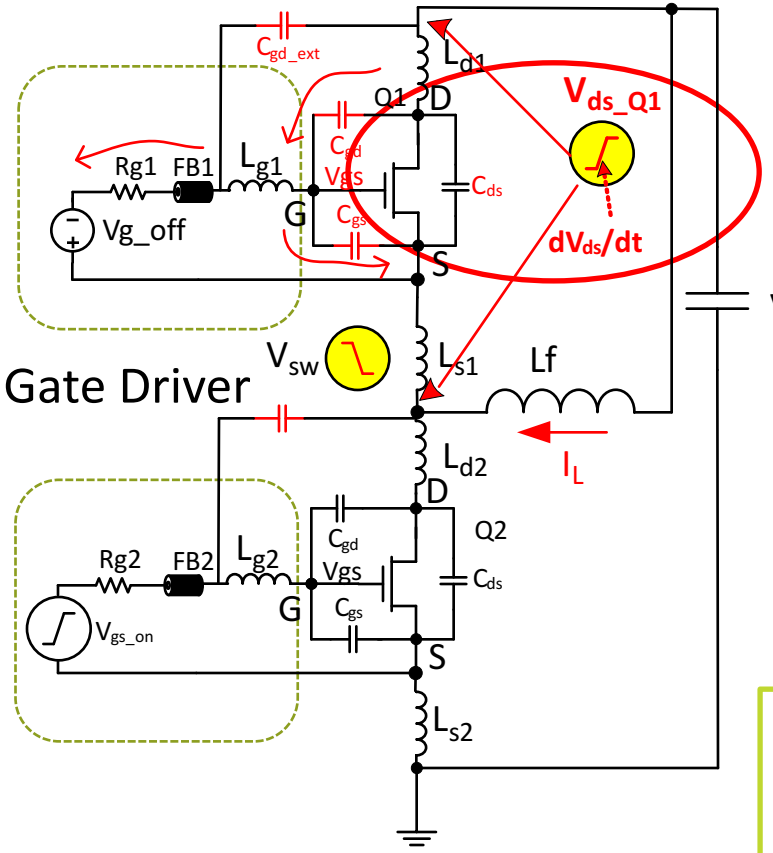


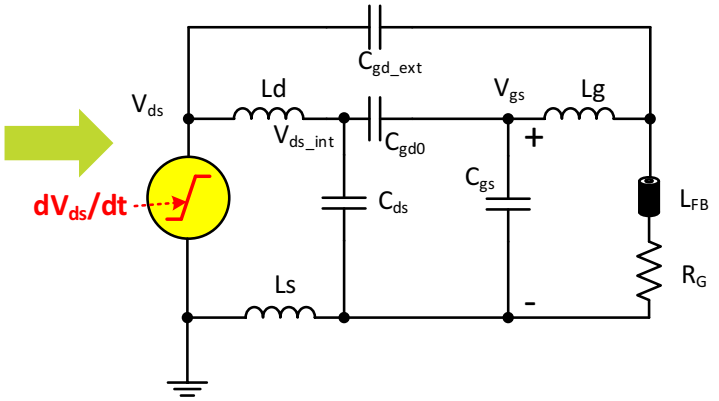
- If V_{GS} is pulled above the threshold voltage V_{TH}, the device will operate in the linear region with transconductance g_m, which can be defined in below equation:

$$I_D=(V_{GS}-V_{TH})*g_m$$

- The large gain in the feedback loop that includes external stray capacitance Cgd_ext can then create a sustained oscillation

The feedback loop transfer function

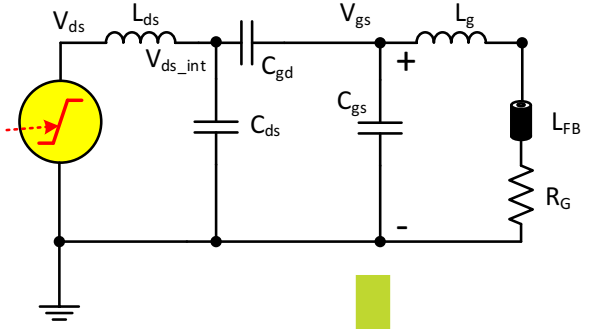




Simplified

$L_{DS} = L_D + L_S$

$C_{GD} = C_{GD0} + C_{GD\_EXT}$

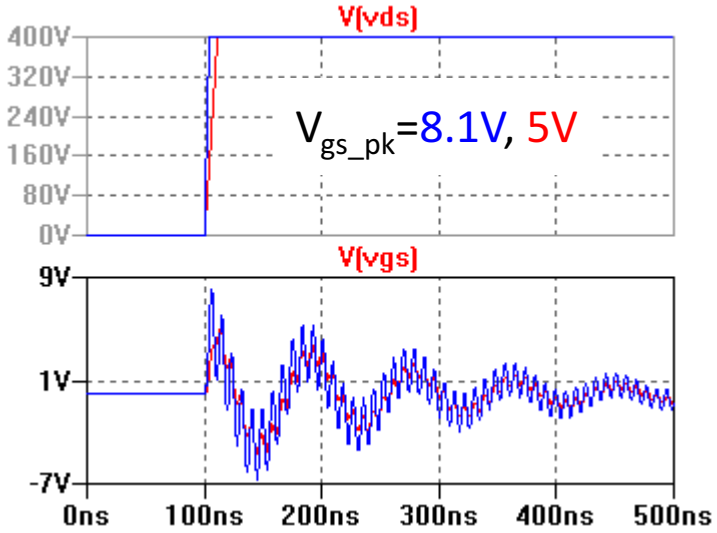


$$F(s) = \frac{V_{gs}(s)}{V_{ds}(s)} = sL_{ds} + \frac{s^2 L_{FB} C_{iss} + sR_g C_{iss} + 1}{s^3 L_{FB}(C_{iss}C_{DS} + C_{GS}C_{GD}) + s^2 R_g (C_{DS}C_{iss} + C_{GS}C_{GD}) + sC_{oss} + 1}$$

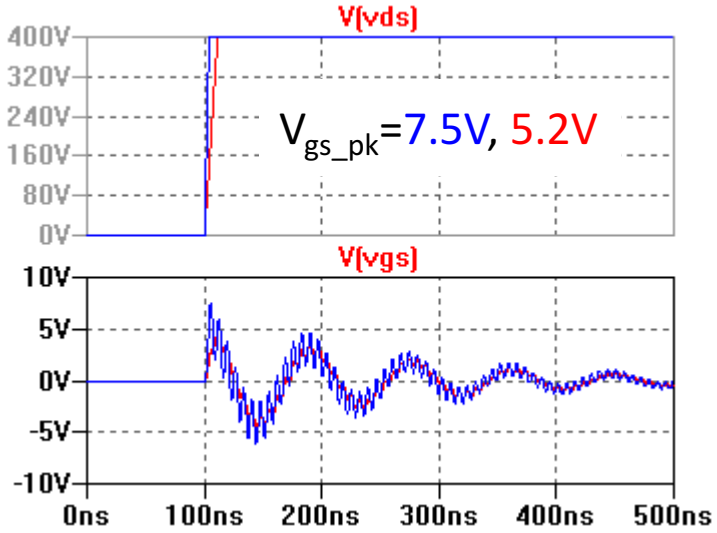
Where: $C_{iss} = C_{GS} + C_{GD}$, $C_{oss} = C_{DS} + C_{GD}$, and $L_{ds} = L_d + L_S$

Comparing ringing amplitude

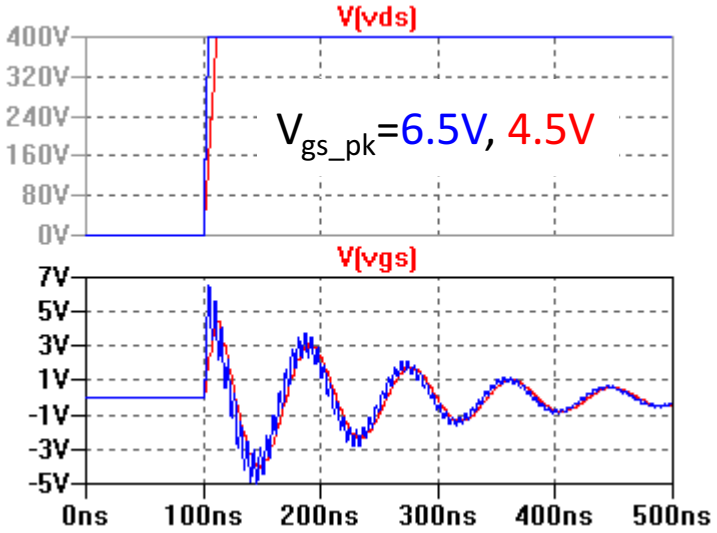
R_{G_OFF}=1Ω, C_{GD_EX}=2pF
Lead_length=15mm (7.5nH)



R_{G_OFF}=1Ω, C_{GD_EXT}=2pF
Lead_length=10mm (5nH)



R_{G_OFF}=1Ω, C_{GD_EXT}=2pF
Lead_length=5mm (2.5nH)



- Comparing blue and red curves, higher dV/dt increases the amplitude of the V_{GS} ringing
- Comparing different parasitic inductances, higher inductances increases the amplitude of the V_{GS} ringing

Red : dV_{DS}/dt=40V/ns
Blue : dV_{DS}/dt=100V/ns

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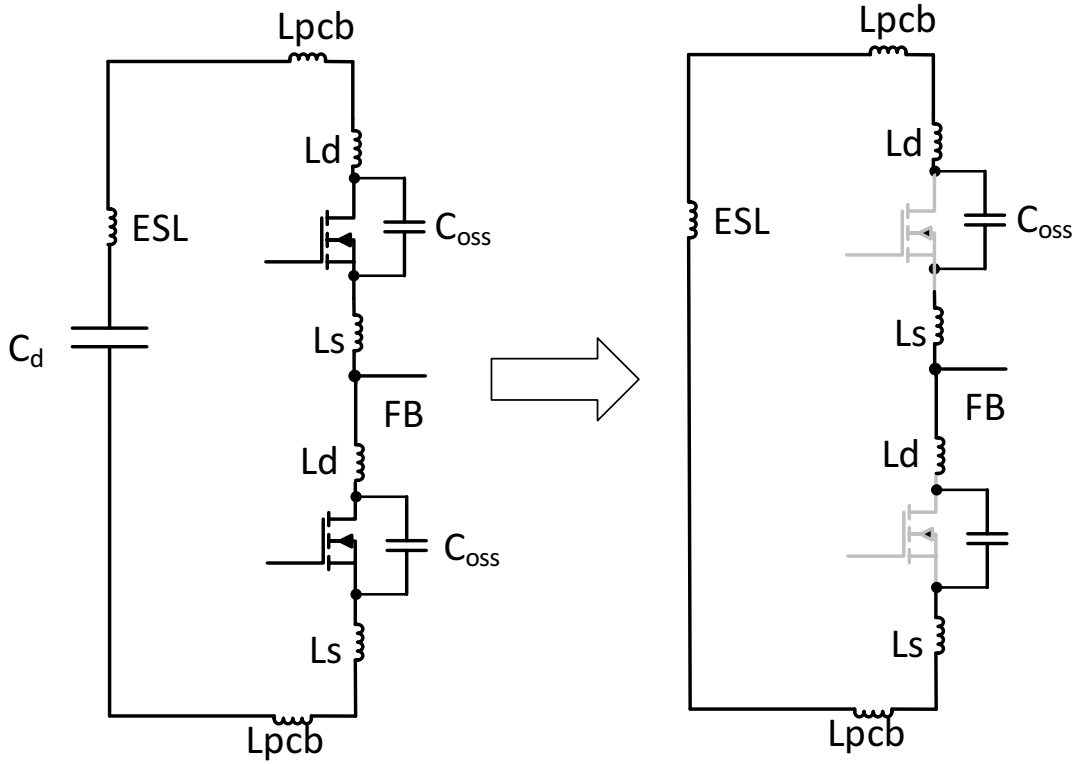
To suppress the sustained oscillation

- Required
  - Optimize PCB layout
  - Use a ferrite bead in the gate
- Highly recommended
  - Add a ferrite bead to the drain
    - Improves efficiency because excessive ringing is lossy
- Optional
  - Add negative Vg_off voltage
  - Reduce the turn-on dv/dt
  - Add an RC snubber to damp the ringing energy
    - Slightly reduces efficiency

NOTE: The above can apply to a single-ended converter with very fast switching

Choosing a Drain Ferrite Bead

Example: Bridge circuit

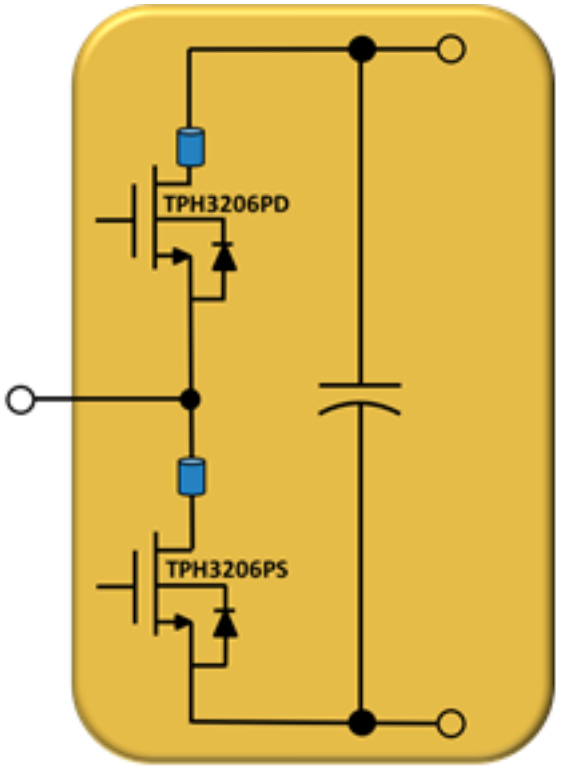


- The equivalent LC resonant loop that largely determines the power loop oscillation frequency

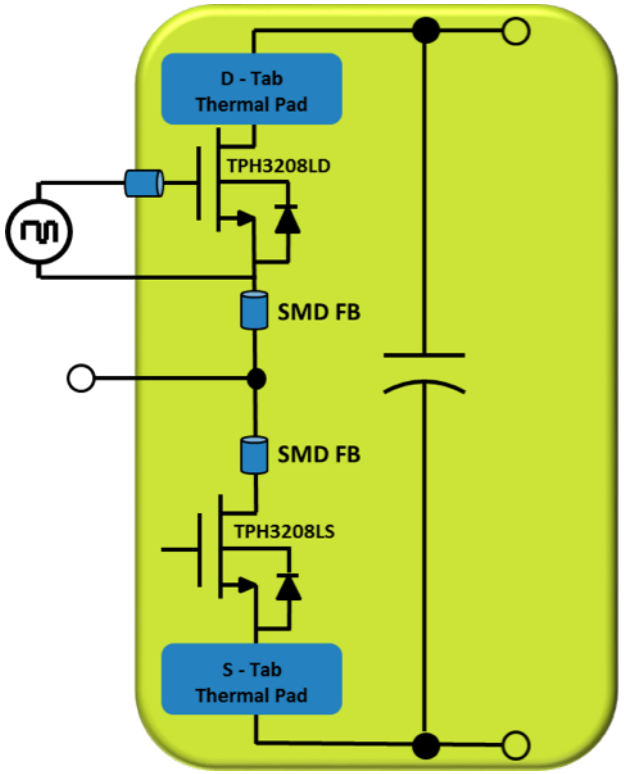
$$L = 2*L_D + 2*L_S + ESL + L_{PCB} + L_{WIRE}$$

$C = C_{OSS}$, (one C_{OSS} is bypassed when device is conducting)

Adding the ferrite bead into the circuit



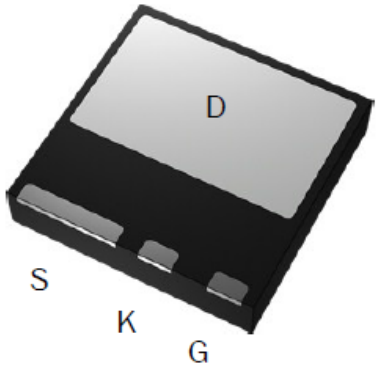
'Ring' (through-hole) type of the ferrite bead can be placed on through-hole type device's D pin



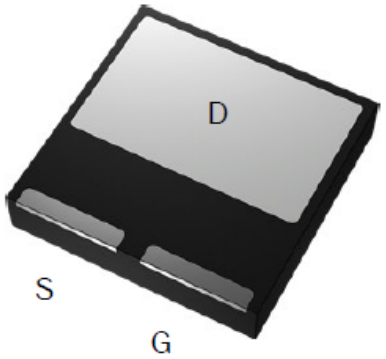
SMD type of ferrite bead should be placed on PCB without interfering with the heat dissipation from the large pad (drain for TPHxxx**LD** part, source for TPHxxx**LS** part)

Transphorm PQFN Package Variations

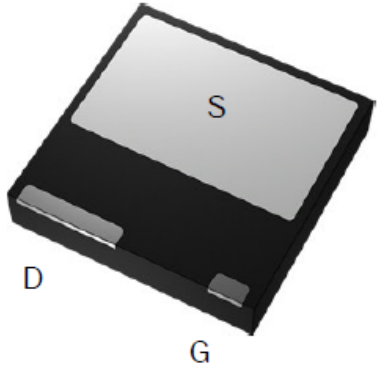
TPH3208LD
8x8 PQFN
(bottom view)



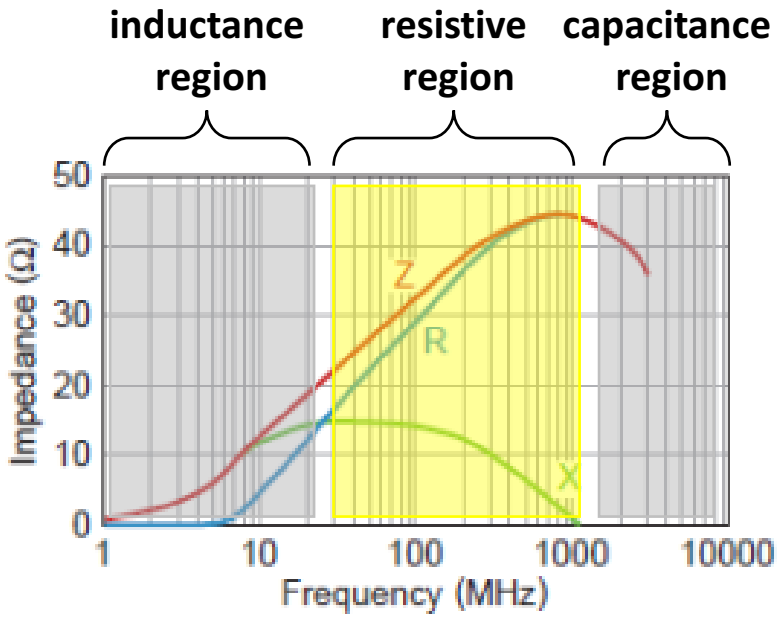
TPH3208LDG
8x8 PQFN
(bottom view)



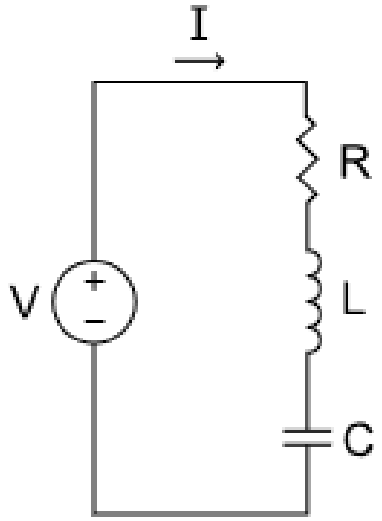
TPH3208LS
8x8 PQFN
(bottom view)



Choose a ferrite bead as a damping resistor at the ringing frequency (50-200MHz)



Choose the ferrite bead that **R>X** @50-200MHz, so the ferrite bead shows more resistive than inductive in this region



For a series LCR circuit, the damping factor is given by:

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}}$$

For critical damping, R should be:

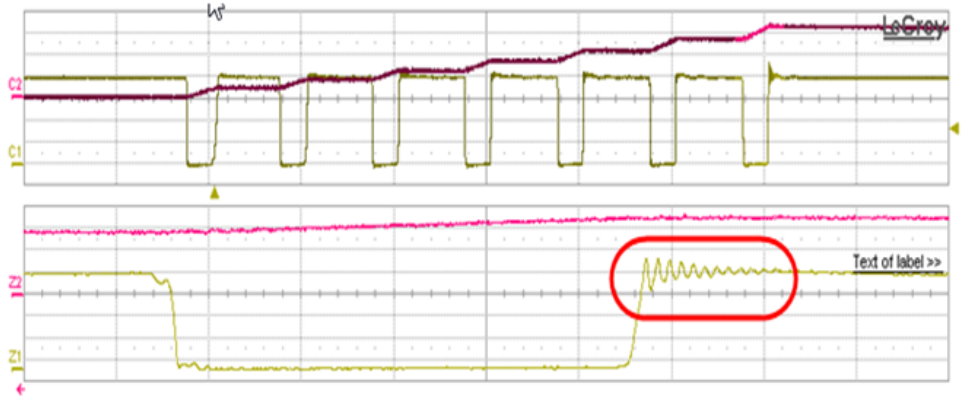
$$R = 2\zeta\sqrt{\frac{L}{C}} = 2 * 1 * \sqrt{\frac{25nH}{110pF}} = 30\Omega$$

So use a bead with >30Ω@100MHz for each device

Verifying the result

Note the ringing

NO DRAIN BEAD



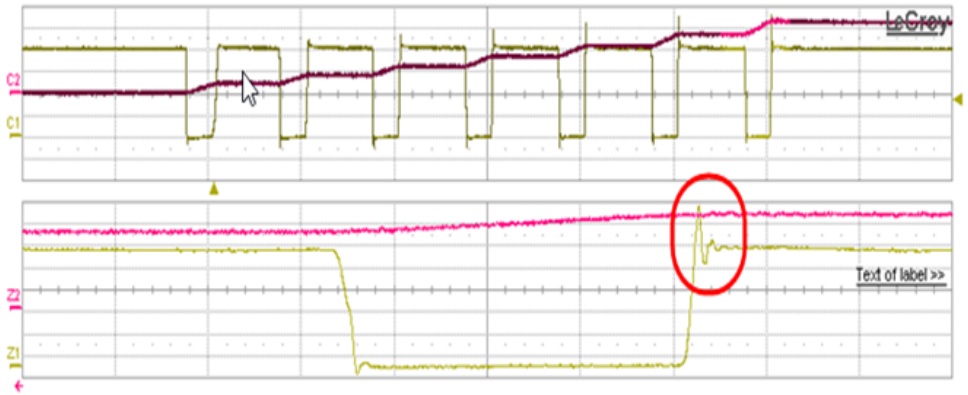
Choke current

Half-bridge output voltage (low-side V_{DS})

ZOOM of above

Note the ringing is well damped

WITH DRAIN BEAD

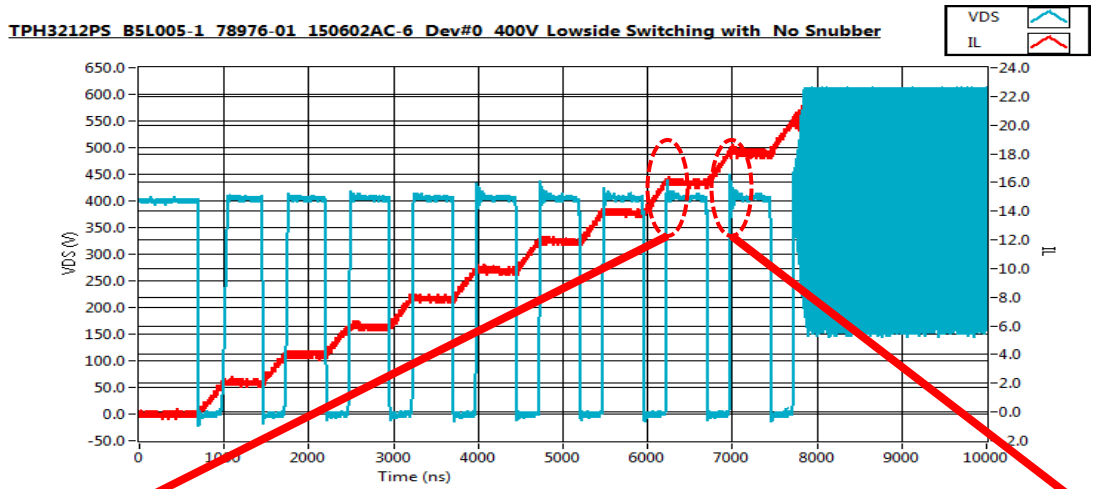


Choke current

Half-bridge output voltage (low-side V_{DS})

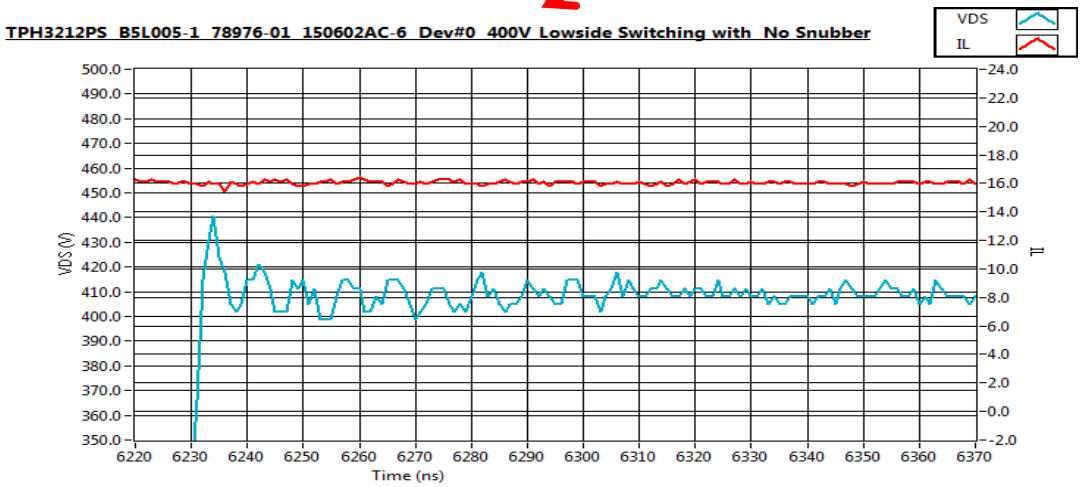
ZOOM of above

TPH3212 HB low side switching w/o FB

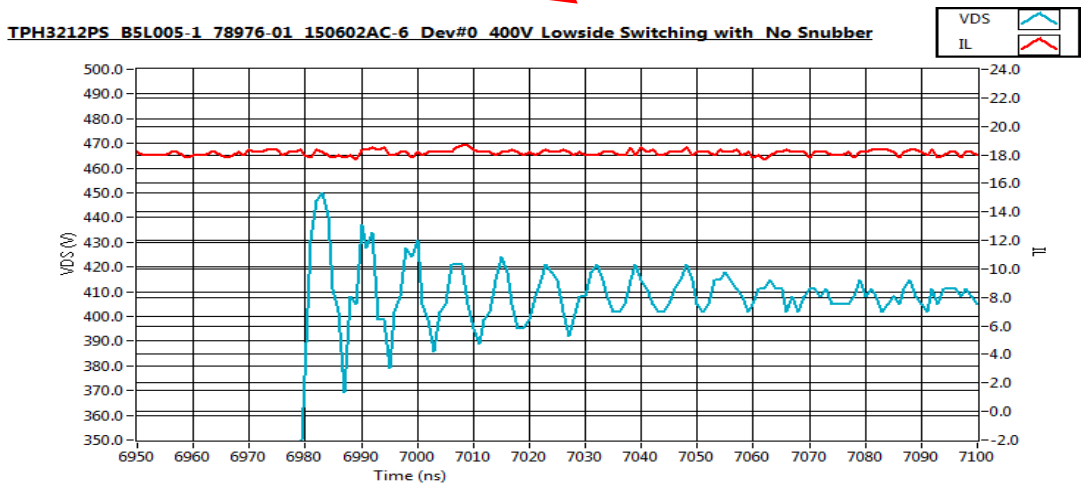


Turn off at 20A, oscillate

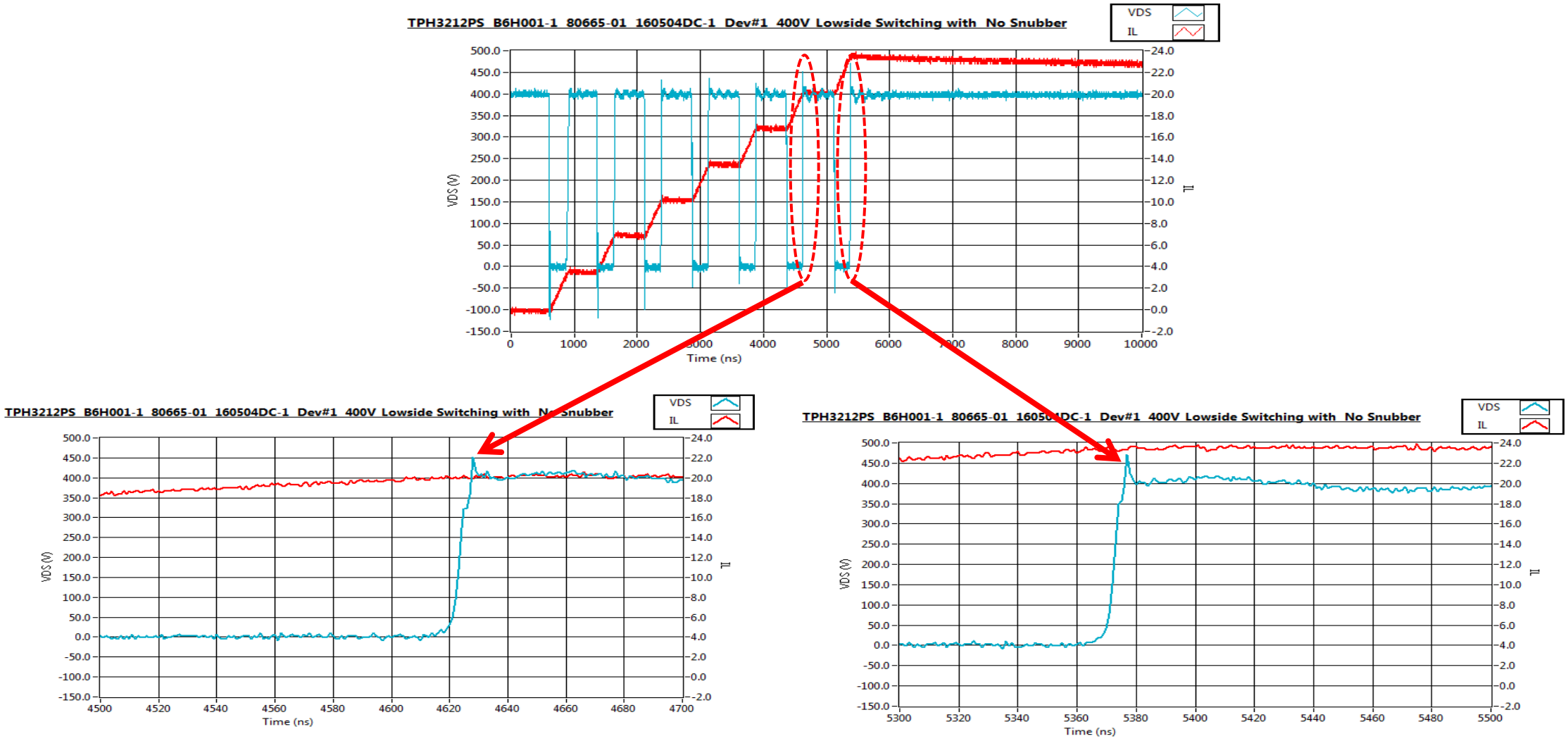
Turn off at 16A, voltage spike damped to <20% after 3 cycles: **Stable**



Turn off at 18A, voltage spike damped to >20% after 3 cycles: **Almost unstable**



TPH3212 HB low side switching w/ FB



Turn off at 20 and 24A, no ringing: **Stable**

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V_{TDS} rating

- Using a drain ferrite bead does increase the drain spike voltage
- However, all Transphorm devices are specified with V_{TDS} (transient V_{DS}) which is 150V higher than the rated max DC V_{DS}
- Transphorm devices are guaranteed to operate safely under repetitive spike voltages within the datasheet specification, making it more suitable for the drain ferrite bead solution

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TPH3212PS

Absolute Maximum Ratings (T_C=25°C unless otherwise stated)

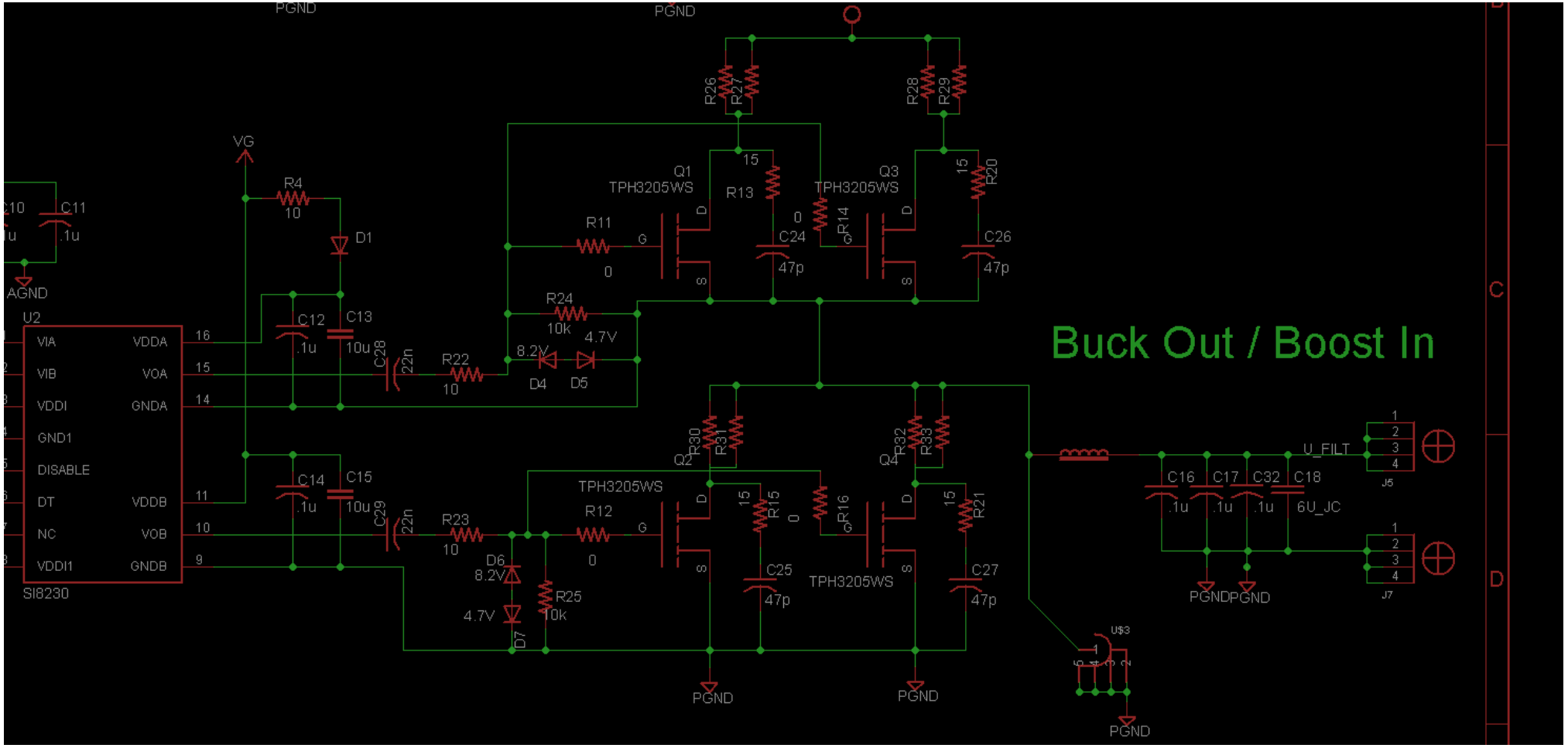
Symbol	Parameter		Limit Value	Unit
$I_{D25°C}$	Continuous drain current @T_C=25°C [a]		26.5	A
$I_{D100°C}$	Continuous drain current @T_C=100°C [a]		16.5	A
I_{DM}	Pulsed drain current (pulse width: 10µs)		120	A
V_{DSS}	Drain to source voltage		650	V
V_{TDS}	Transient drain to source voltage [b]		800	V
V_{GSS}	Gate to source voltage		±18	V
$P_{D25°C}$	Maximum power dissipation		104	W
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{CSOLD}	Soldering peak temperature [c]		260	°C

Thermal Resistance

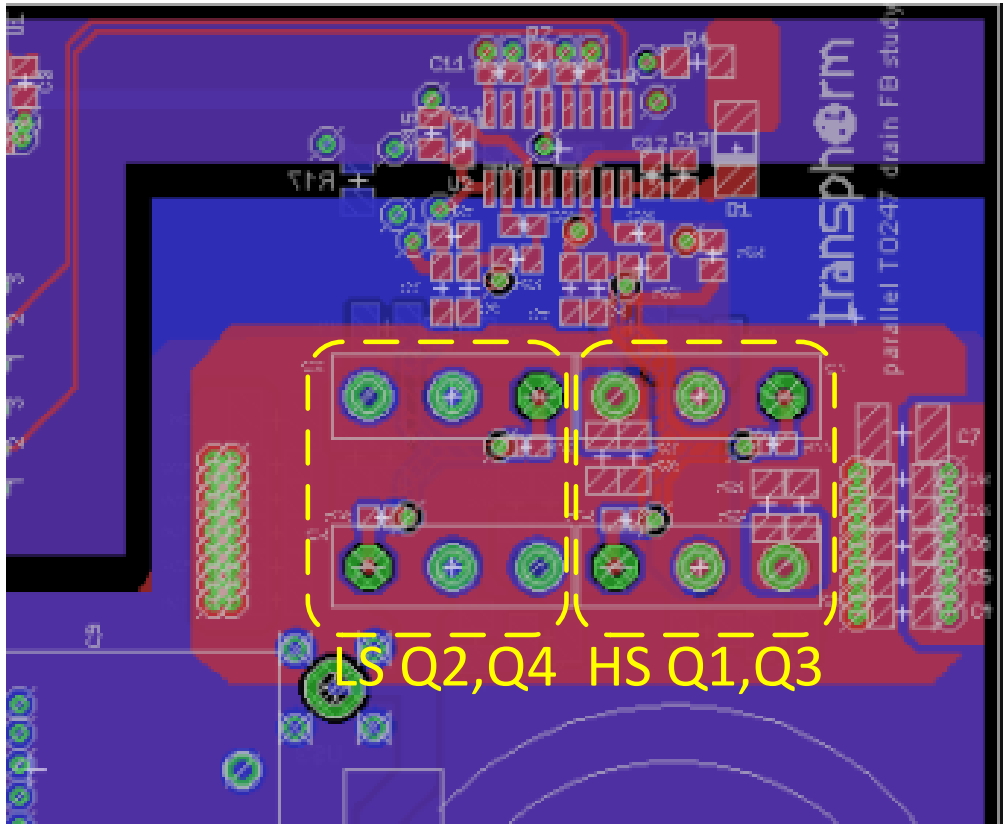
Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Junction-to-case	1.2	°C/W
$R_{\theta JA}$	Junction-to-ambient	62	°C/W

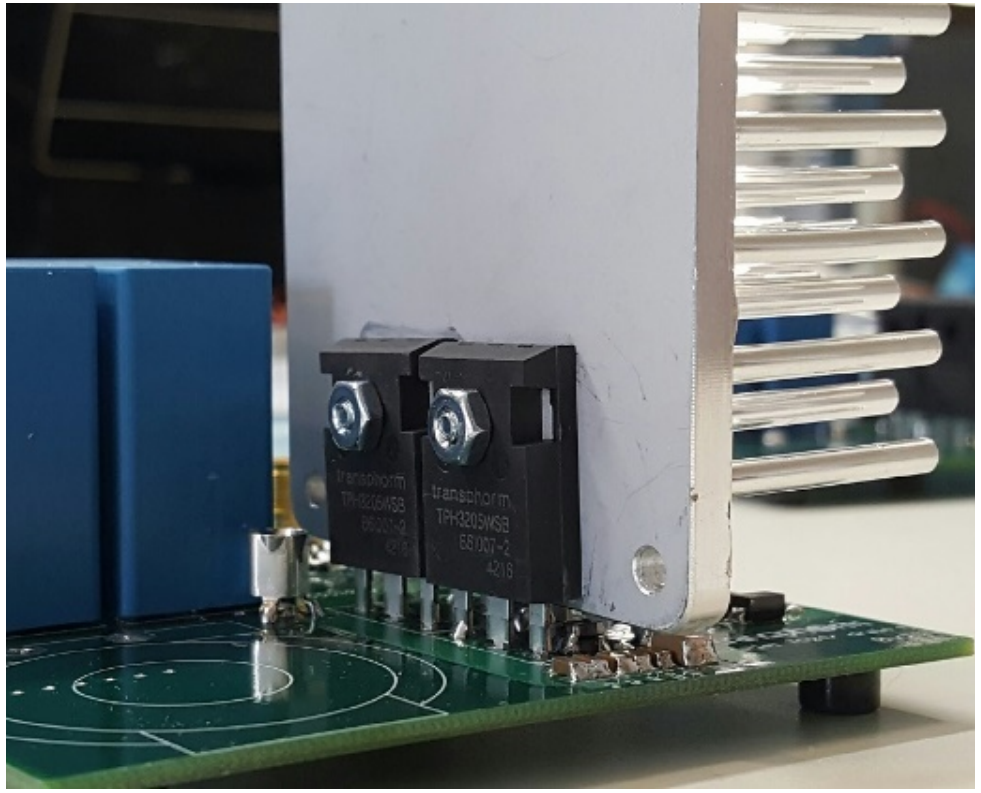
Notes:
a. For high current operation, see application note AN0009
b. In off-state, spike duty cycle D<0.01, spike duration <1µs
c. For 10 sec., 1.6mm from the case

Paralleling 650V/52mohm GaN with FB



Layout with TO247 Packages





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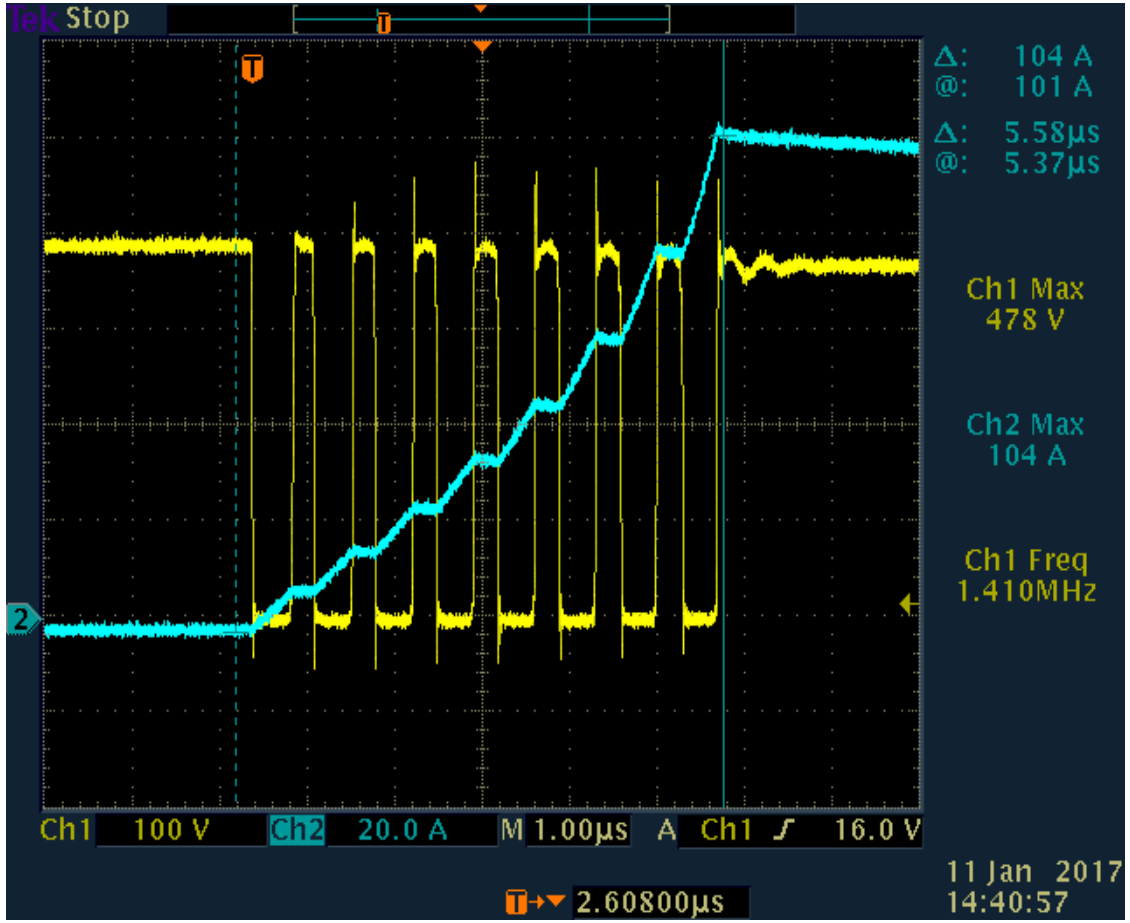
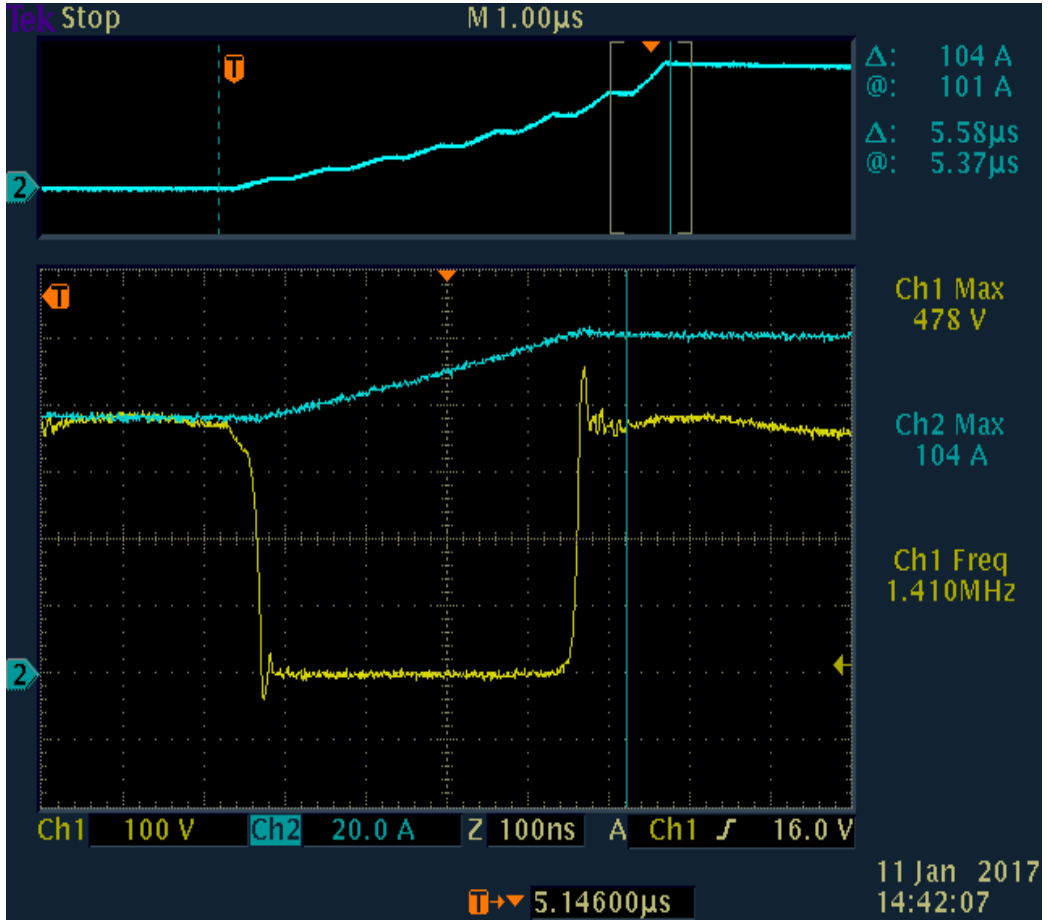
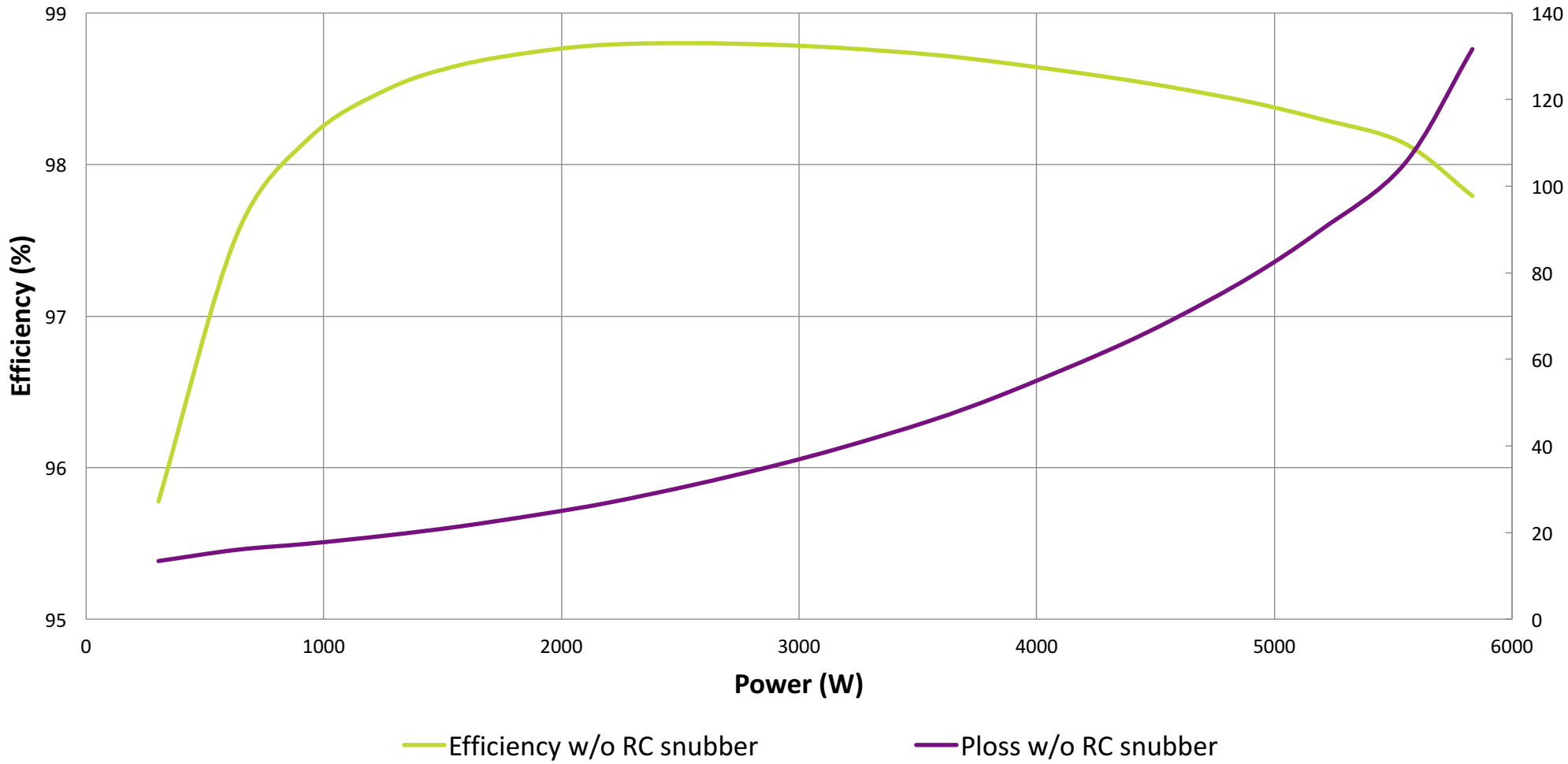
Switching 400V/100A with Clean Waveform





200V:400V Boost Converter
5.5kW and 98.8% Peak Efficiency



Silicon Valley Center of Excellence

Design Tools: Evaluation kits, reference designs, simulation models (SPICE)

Support: Global field applications team, Q+R testing, system component selection analysis, technical marketing

Education: EMI control methods, high power app concepts, optimization techniques, topology comparisons, etc.

Technical Library: Application notes, design guides, PCB layouts, schematics, technical white papers

Thank You!

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Highest Performance, Highest Reliability GaN