# PQFN GaN FETs Paralleling PCB Application Note

## 1. Introduction

Trasphorm's PQFN (Power Quad Flatpack No Lead) package incorporates a DPC (Direct Plated Cu) substrate and a Cu lead frame encapsulated in a green molding compound for bottom electrical connection and thermal contact to printed circuit board. It provides high lateral electrical isolation and excellent heat dissipation in applications similar to a D2Pak but in a thinner form factor [1]. The new generation 650V/70mΩ PQFN packaging devices TP65H070LxG have been released, where the "X" is "S" or "D" meaning source tab or drain tab, respectively. For the traditional Si-MOSFET, there is only drain metal tab PQFN device as the bottom of the die is always drain terminal. GaN FETs have much higher dv/dt switching speed. For the bridge applications, if both high side and low side devices are drain tab ones and connected to the large copper PCB for heat dissipation, the low side drain tab will be the switching node. High dv/dt potential change on this copper area will behave like an antenna to radiate high frequency noise, or high the dv/dt will couple through the capacitance between PCB and heatsink or other signal layers to generate common mode noise current, resulting in Electromagnetic compatibility (EMC) issue or circuit malfulction. In order to solve this issue, it is better to choose source tab device for low side and drain tab device for high side. As a result, the tabs will connect to either power ground or high voltage DC rail where there are no high dv/dt switching, and the large copper plates helps build up decoupling capacitance to suppress the voltage spikes.

The generation III devices provide 4V threshold gate voltage and better switching performance. For achieving higher power requirement, 2x PQFN in parallel is necessary. In this application note, the combination with LDG FETs on high side and LSG FETs on low side in paralleling will be discussed.

## 2. Cuicuit Parameters and PCB Layout for PQFN Paralleling

It is similar to TO247 circuit, the symmetrical PCB layout is important for successfully paralleling [2]. Figure 1 shows the PQFN paralleling half bridge circuit schematic, in which the 2x TP65H070LSG and 2x TP65H070LDG are directly paralleled. Two Si8271 single device drivers are used to drive high side and low side devices as it provides >150V/ns CMTI capability and separated turn-on and turn-off pins for flexible on/off Rg setting. In this application Rg_on and Rg_off are set to 10 Ω, and a 15 Ω additional Rg is added to the gate of each device. A 220 Ω@100MHz gate ferrite bead (P.N.: MPZ1608S221ATA00) is used to suppress the gate noise, and the gate voltage is 0 - 12V. The high current ferrite beads are used to connect high side and low side devices. 2x 8.5A 30Ω@100MHz ferrite beads (P.N.: BLM21SN300SZ1D) connect to the high side source terminals, and another two connect to the low side drain
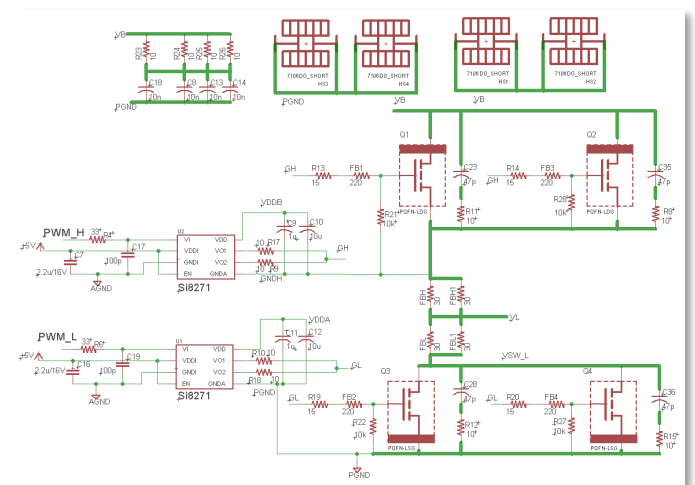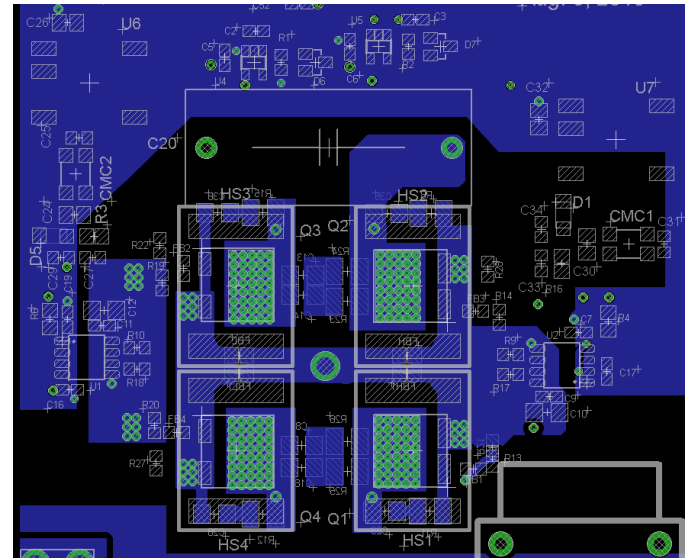


**Figure 1. PQFN paralleling half-bridge circuit**

terminals. In this way, the high side drain tab and low side source tab connecting to the big copper plates for heat dissipation will not be broken. A 47pF+10Ω RC snubber putting closely to each device is to reduce the turn-off ringing. A solderable PQFN/D2-PAK heatsink (P.N.: 7106DG) is selected for heat dissipation. This heatsink is good for 2~2.5kW totem pole PFC application. For even higher power application, larger heatsink mounted on the bottom should be applied, the heat will transfer to the bottom layer through the thermal vias. Figure 2 shows the PCB layout for each layer. The circuit picture with boost inductor and heat sinks are shown in Figure 3.



(a)



(b)



(c)

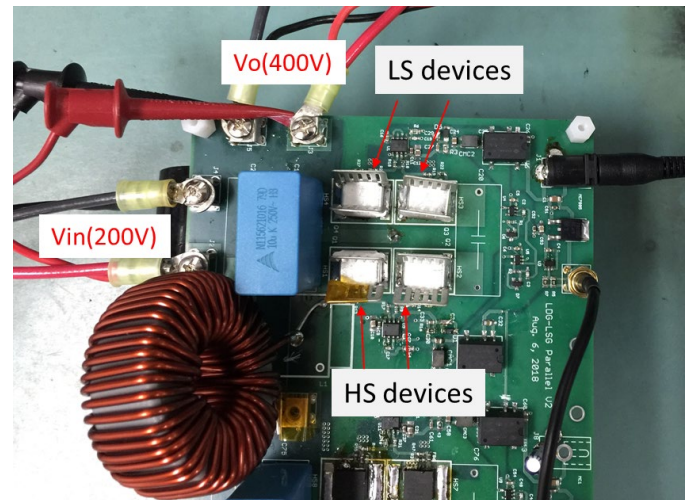Figure 2 Paralleling PQFN half bridge circuit layout. (a) Top layer, (b) Middle layers, (c) Bottom layer.
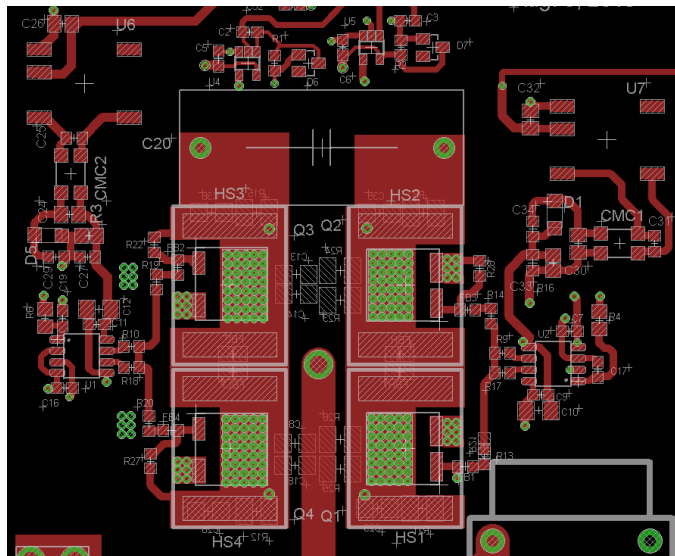


Figure 3 PQFN half bridge circuit picture

## 3. High Current Hard-switching Test

High side and low side hard switching tests are conducted for circuit stability verification. Figure 4 and Figure 5 show the high side and low side switching test waveforms at 400V, respectively. It can be seen that the voltage ringing is suppressed, and there is only one voltage spike due to the ferrite beads. With 25 Ω gate resistor, the turn-on dv/dt is 44V/ns, and turn-off dv/dt is 57V/ns at 50A. The overshoot voltage spike is 466V.

(a)



(b)
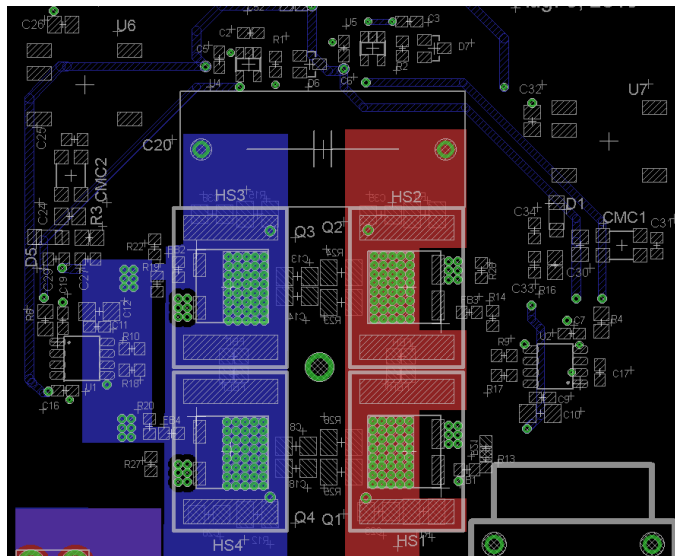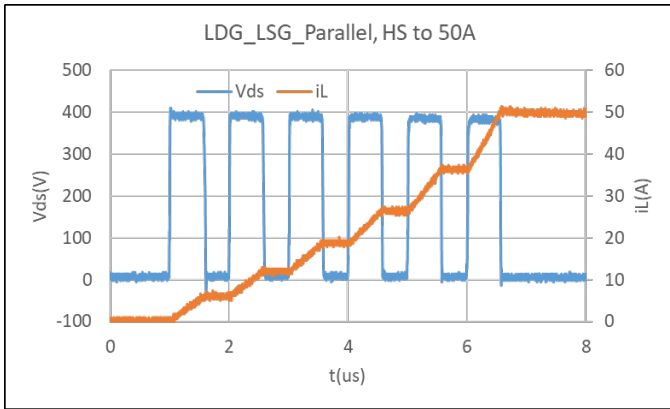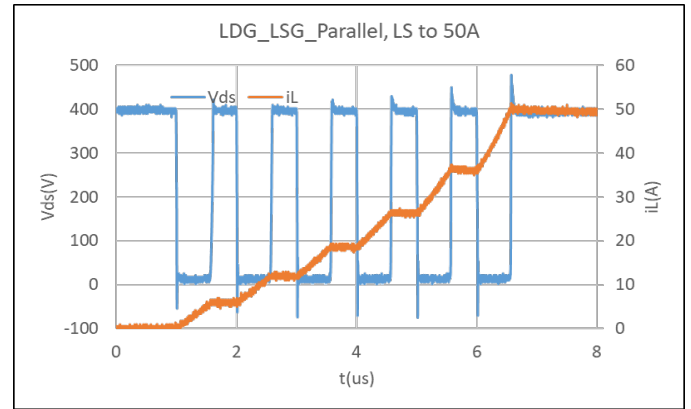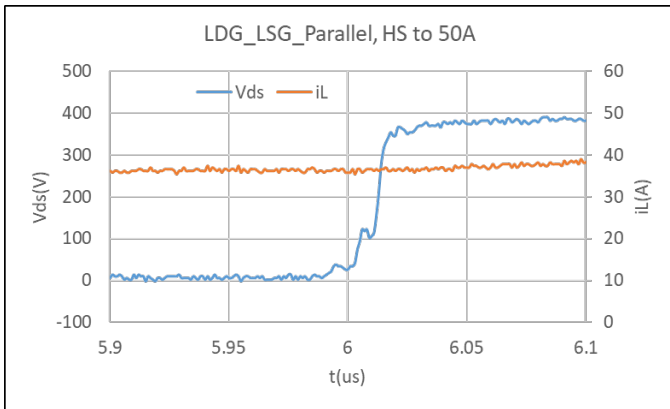


(c)

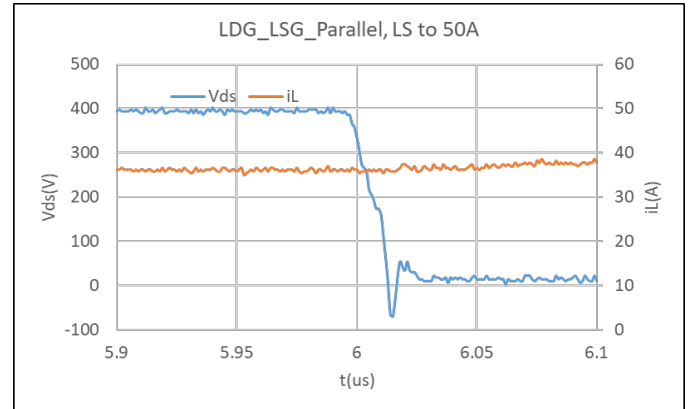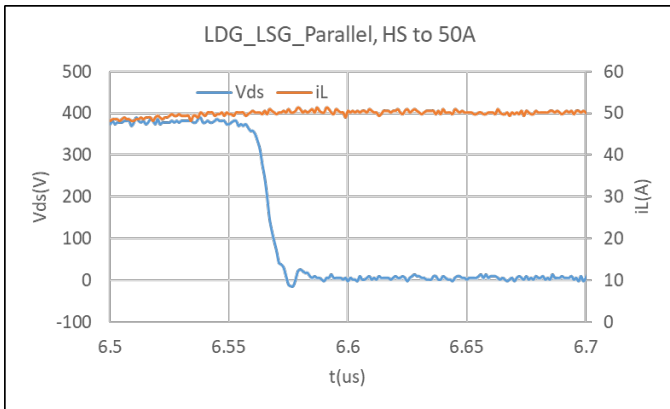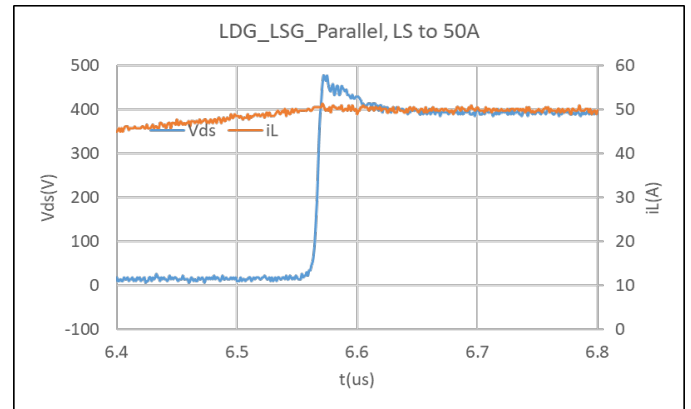Figure 4 High side device hard switching to 50A (a) 50A switching waveform, (b) the last turn-on switching waveform, (c) the last turn-off switching waveform



(a)



(b)



(c)

Figure 5 Low side device hard switching to 50A (a) 50A switching waveform, (b) the last turn-on switching waveform, (c) the last turn-off switching waveform

## 4. Efficiency Measurement and Calculation

The efficiency is tested by configuring the half-bridge in synchronous rectification boost mode. The input voltage is 200V, output voltage is 400V and the circuit is

switching at 50kHz or 100kHz with a 330 µH MPP core inductor. Figure 6 shows the efficiency curves, and the efficiency is over 99% at >1.25kW@50kHz and the efficiency is over 98.8% at >1.5kW@100kHz. The power rating at 100kHz is limited at 2.2kW due to the low side device case temperature rising to around 100 °C, as shown in Figure 7. However, in the totem pole PFC application or full bridge inverters, the high side and low side devices will be operating in hard switching mode every half cycle, the switching loss can be evenly shared, therefore the temperature rising will be lower than boost converter. With the small SMD mounted heat sink, the paralleled PQFN is good to run over 2.5kW at the condition of high line and 100kHz switching frequency.
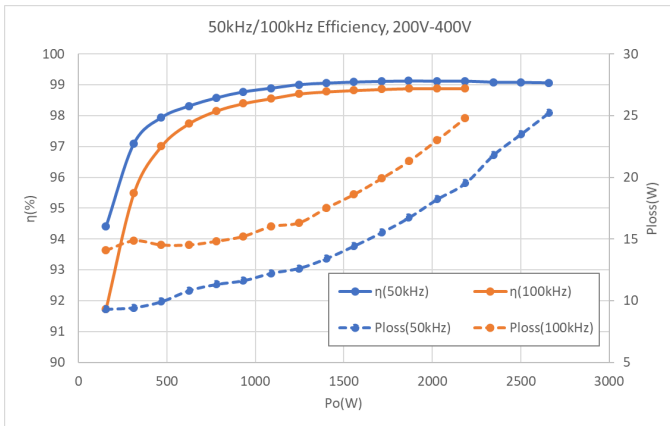


Figure 6 Efficiency Measurement at 200Vin-400Vo, 50kHz and 100kHz
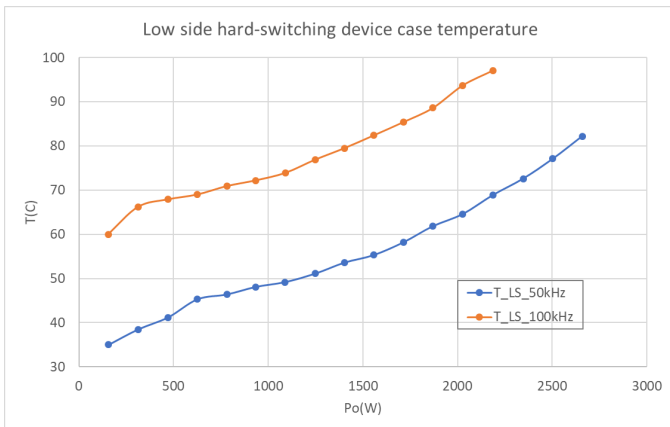


Figure 7 Low side device case temprature at 100 CFM air flow condition

The converter efficiency can also be estimated. The key part is to estimate the GaN FETs turn-on switching loss

as the turn-off loss is pretty small and it is relatively constant with no change with the current increasing. We can use the switching waveform with low side Vds and inductor current to do the calculation.
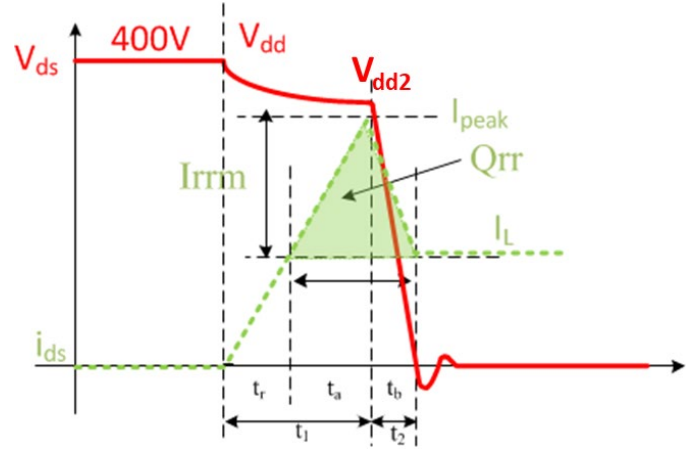


Figure 8 A typical turn-on Vds and Ids waveform

As shown in Figure 8, a typical turn-on waveform shows how the voltage and current change. In the first stage t1 period, the drain current will increase to the Irrm, and voltage across the drain and source will drop to Vdd2 due to the $L_{stray}$*di/dt, in the second stage t2 period, the Vds voltage will drop to zero and current goes down to the inductor current. We could not measure the drain current using regular low bandwidth current probe, but with the voltage and inductor current waveform and datasheet, we know Vdd, t1, t2, iL, Qrr. The intermediate variable tr, ta, Irrm can be calculate as:

$$t_a = \frac{-(i_L t_2 + 2Q_{rr}) + \sqrt{(i_L t_2 + 2Q_{rr})^2 + 8i_L t_1 Q_{rr}}}{2i_L} \qquad (1)$$

$$t_r = t_1 - t_a \qquad (2)$$

$$i_{rrm} = \frac{2Q_{rr}}{t_a + t_b} \qquad (3)$$

The turn-on loss can be described:

$$E_{on} = \frac{1}{2}V_{dd}i_L t_r + V_{dd}\left(i_L + \frac{1}{2}i_{rrm}\right)t_a + V_{dd}\left(\frac{1}{2}i_L + \frac{1}{3}i_{rrm}\right)t_b \qquad (4)$$

Figure 9 shows the waveform at 5.2A turn-on. t1, t2 and Vdd2 are measured 9.6ns, 4.4ns and 220V, respectively, and the Qrr is 180nC@400V. The turn-on loss can be then estimated 58uJ. The Eon vs IL curve can be plotted in Figure 10, and the fitting equation is obtained.
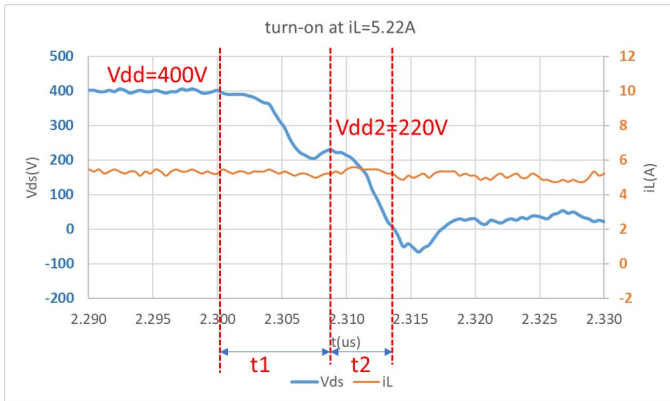
Figure 9 Vds and IL waveforms at low side device turn-on at 5.2A



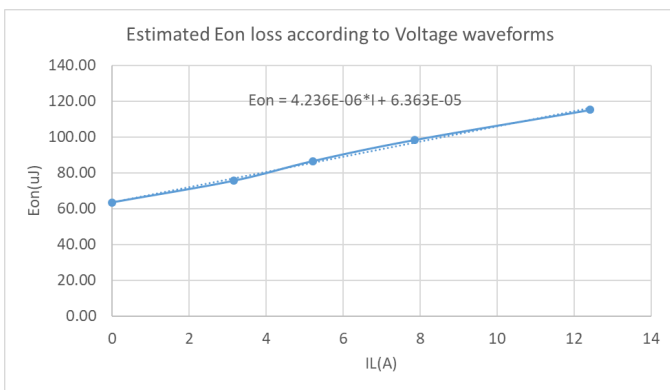Figure 10 The estimated turn-on energy for 2x70mΩ GenIII vs iL at 400V

The turn-off loss and high side device transition loss is small and constant around 23uJ. By carefully calculating other components losses, the converter efficiency curve can be plotted and the comparsion with measured result is shown in Figure 11. It is seen that the efficiency curve well match the measured curve. At light load, since the current drops to zero but Vds is not fully charged, the turn-on process is different from the hard-switching waveform, the estimated loss is a slightly lower. The loss breakdown is plotted in Figure 12 showing the losses on inductor, input/output capacitor, RC snubber circuit, and devices switching and conduction losses.
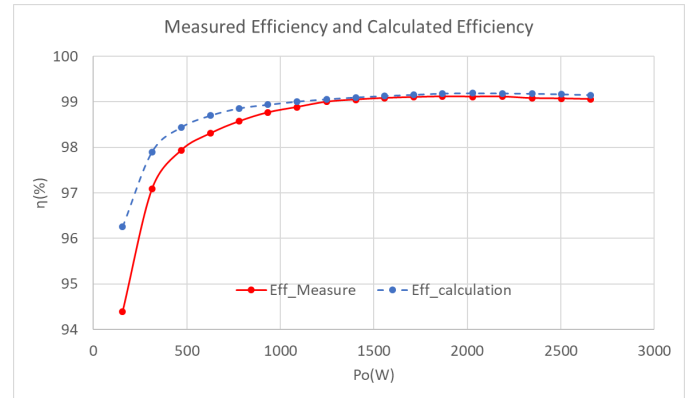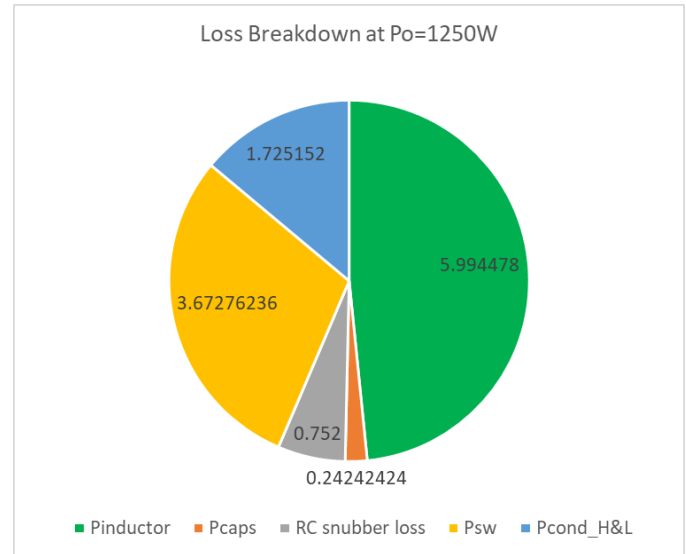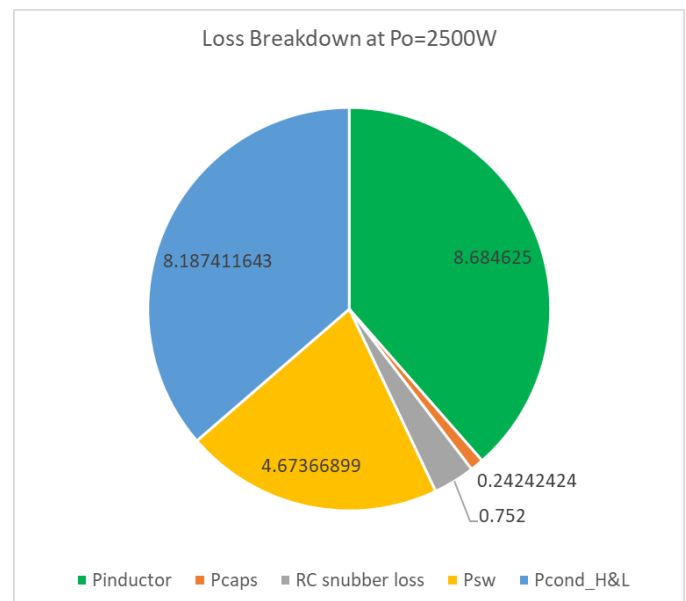


Figure 11 The measured efficiency vs estimated efficiency curve.



(a)



(b)

Figure 12 Losses breakdown at 1.2kW Po and 2.5kW Po, fsw=50kHz.

## Reference

[1] "AN0007: PQFN88 Lead-free 2nd Level Soldering Recommendations for Vapor Phase Reflow". Available: www.transphormusa.com.

[2] "AN0010: GaN FETs in Parallel Using Drain Ferrite Beads and RC Snubbers for High-power Applications". Available: www.transphormusa.com.