Paralleling GaN HEMTs for Diode-free Bridge Power Converters

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Abstract— **GaN devices have superior performance over Si-based devices, and high voltage normally-off GaN HEMTs with cascode structure have been available for industry application as they can be easily driven by mature commercial Si-MOSFET drivers. Due to the very fast switching speed, the PCB layout and driver circuit design should be very careful to keep the parasitic parameters as small as possible. Paralleling semiconductor devices is an effective and simple way for higher power application. It is very challenging to parallel GaN HEMTs in hard-switching bridge power converter application, especially for discrete leaded package devices. However, leaded packages are still dominant in industrial applications because of their simplicity for PCB assembly and capability for a wide variety of heat-sinking techniques. In this paper, a solution to paralleling GaN HEMTs for diode-free bridge power converters is proposed, and GaN device driver design is discussed. The partial phase method is also suitable for the low power application to improve the efficiency. Simulations of driving circuit and experimental results on a 5 kW half bridge operating in synchronous boost mode with 4 paralleling GaN HEMTs are provided for validation.**

Keywords—GaN; HEMT; leaded package; parallel; bridge

I. INTRODUCTION

Currently widely used in LEDs, Gallium Nitride (GaN) is the next generation in power electronics. The GaN high electron mobility transistor (HEMT) combines low switching and conduction losses, offering reduced energy loss of more than 50 percent compared to conventional silicon-based power conversion designs. Transphorm Inc. has established the industry's first qualified 600-V GaN device platform with its TPH3006 GaN HEMT. The TO-220-packaged device features $R_{ds(on)}$ of 150 mΩ, Q_{rr} of 56 nC and high-frequency switching capability that enables compact lower cost systems [1], as shown in Fig. 1. Not only applicable for high frequency DC-DC converter applications [2], GaN HEMTs are also promising for replacing Si-IGBTs in AC-DC/ DC-AC applications, such as PFC, PV inverter and motor drive applications [3-5].

Two types of TO-220 600-V GaN HEMTs are provided which have Source Kelvin Tab and Drain Tab, respectively. Soldering the tab directly to the PCB is a good way for eliminating the lead parasitic inductance so as to reduce ringing on gate and switching node [6], but it is not widely used in industry due to the issues of reflow soldering and heat dissipation limitation. For the high power application, low thermal resistance heat sinks are necessary to mount on the tabs of GaN HEMTs, and PCB layout with leads connection should be studied. Moreover, paralleling GaN HEMTs is also attractive for high power applications [7-9]. However, it is very challenging for paralleling discrete GaN devices as the parasitic inductance increases with the increasing footprint.

In this paper, a basic half bridge along with driver circuit using discrete GaN HEMTs is analyzed, and then two and 2N devices in parallel are discussed. Simple and robust solution without PCB layout and thermal management limitation is proposed. A partial phase operation mode is also applicable for this method for improving the efficiency at low power.

II. INVESTIGATION OF DRIVING CIRCUIT OF HALF BRIDGE GAN HEMTS

Fig. 2 shows a half bridge circuit schematic with half-

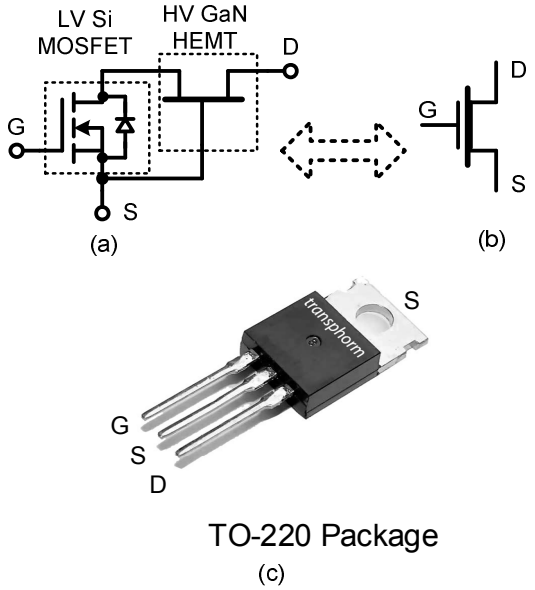
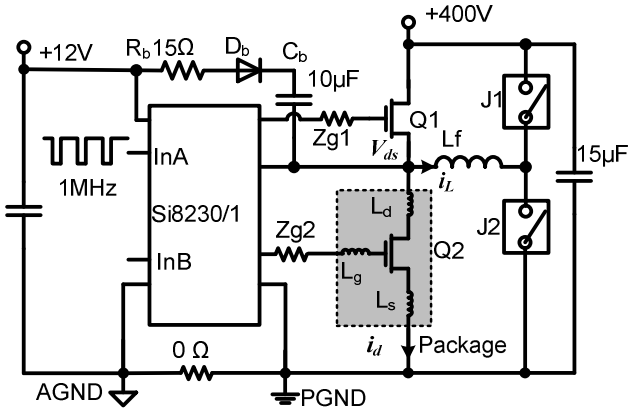
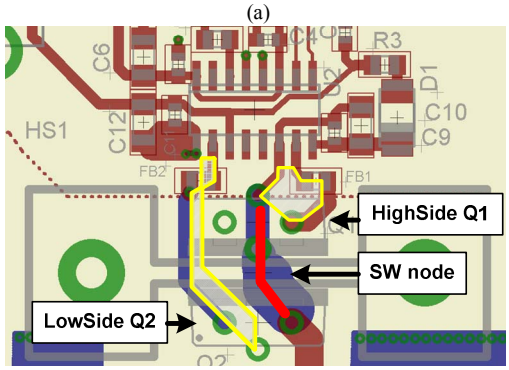


Fig. 1: GaN hybrid HEMT incorporating a LV normally-off Si FET and an HV normally-on GaN HEMT (a) to achieve a combined, normally-off device (b) in a Quiet-Tab TO-220 package (c).

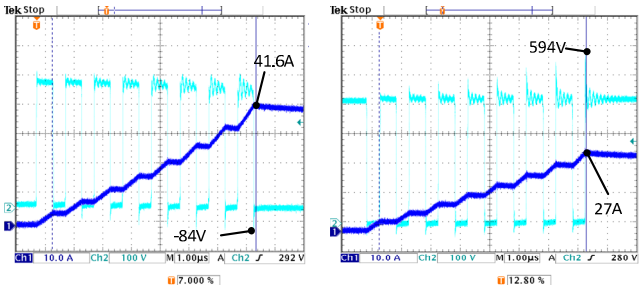


(a)

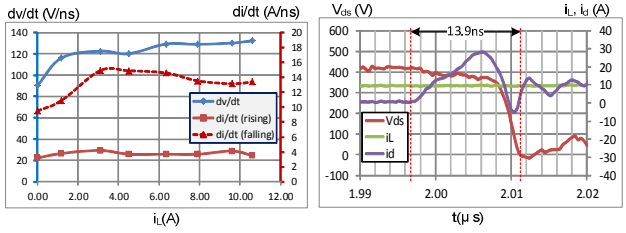


(b)

Fig. 2: Half bridge GaN HEMTs test circuit: (a) schematic, J1 is for low side device hard switching test, J2 is for high side hard switching test; (b) Half bridge test circuit back-to-back 2 layer layout: switching node connection is minimized, while low side gate loop trace is longer than high side.



(a) (b)



(c) (d)

Fig. 3: Multi-pulse hard-switching test, f_{sw} = 1MHz, N_{pulse} = 8, f_{cycle} = 30 ms. (a) High side hard-switching to 41.6 A; (b) Low side hard-switching to 27 A. (c) Dv/dt and di/dt rating from 0 A to 10 A; (d) Cross over time is 13.9 ns at i_L = 10 A.

bridge boot-strap driver. Due to the very high di/dt rating, Si8230/1BB driver from Silicon-Lab is selected as it consists of a half bridge MOSFETs driver and digital isolator, which provides best-in-class noise immunity thanks to its less than 2 pF coupling capacitance [10].

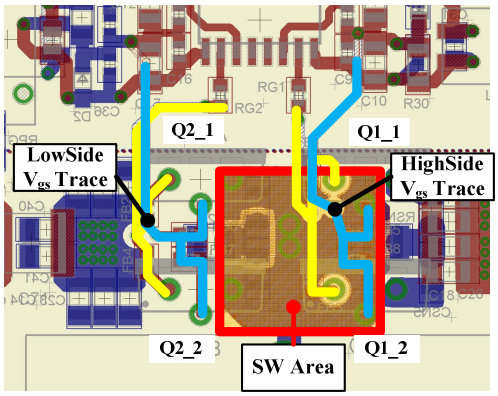
The TO220 package unavoidably adds inductance in the source lead, as shown in Fig. 2 (a). This inductance cannot be further reduced, and so its impact must be recognized and mitigated. The normal expectation when a voltage signal develops across a source impedance is that it will subtract from the gate-drive voltage and slow the turn on. Slowing the di/dt transition by reducing I_g will indeed reduce the corresponding source voltage during that part of the turn-on transient. Using a gate resistor in the place of Z_g in Fig. 2 would accomplish this. A gate resistor will not, however, provide the additional function of limiting slew rate at the switching node: $d(V_{ds})/dt$. This is because the feedback capacitance, C_{rss}, of the cascode combination is so low. Simply choosing a gate driver with a lower output current is a better way to limit I_g and di/dt. It is found that a small SMD ferrite bead effectively opposes such transient current and inhibits coupling of the signal [11], although the voltage waveform on the gate pin is not obviously damped.

A ferrite bead MMZ2012D121B from TDK is selected as Z_g, which has nearly zero dc resistance and 120 Ω impedance at 100 MHz, and a 15 Ω/ 0.5 W resistor as R_b for preventing circuit from impacting by inrush current caused by undershoot voltage spike of high side device switching. Fig. 3 (a) shows the high side device can hard switch at 41.6A with V_{ds} undershoot no more than -100V; Fig. 3 (b) shows the low side device can hard switch at 27A with V_{ds} spikes no more than 600V. The dv/dt and di/dt are over 120 V/ns and 10 A/ns, respectively, which mean the switching speed does not slow down and switching loss will keep low at high switching frequency. Although the back-to-back placement provides a very compact layout, the possible reason that low side device blows up at 31A hard-switching test is the gate circuit loop is larger compared to high side device as shown in Fig. 2 (b).

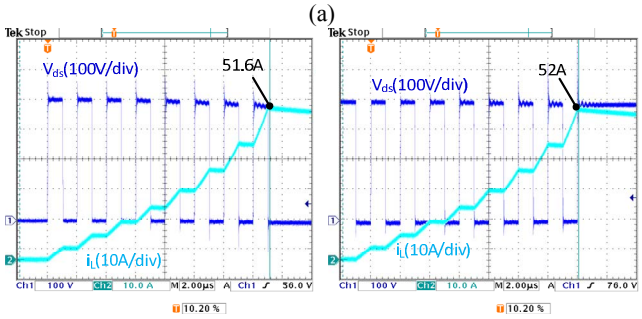
III. Investigation of Discrete GaN HEMTs in Parallel

It becomes more difficult to parallel discrete GaN devices for bridge power converters, because the parasitic inductance and capacitance on PCB layout will increase due to the foot prints' area increasing. In [12], four paralleling GaN HEMTs are proposed for high power boost converter application. The layout is very compact to minimize the parasitic inductance and the driver length should be equal to make the switching time symmetrical. For the half bridge application with GaN HEMTs, the switching stress will be higher than unidirectional boost converter using SiC diodes, so voltage ringing caused by common source inductance is more severe. Since the threshold gate voltage of MOSFET is only 2.1 V, the oscillation voltage spikes due to interference of high side turn off may make the low side device fault turn on. Under this consideration, negative voltage bias on the gate driver is proposed in the

previous research [13].



(a)



(b) (c)

Fig. 4: Half bridge circuit with directly paralleling TO220 GaN HEMTs: (a) compact and symmetrical 4 layer layout; (b) High side hard-switching up to 51.6 A; (c) Low side hard-switching up to 52A.

A. Two devices paralleling

As shown in Fig. 4 (a), a half bridge circuit with 2x devices directly paralleling is presented. In order to make the gate circuits symmetrical to each device, side-by-side layout is selected. It is seen that the gate loop area increases and switching node connection is longer than back-to-back placement, while it is good for the thermal dissipation as the two heat sources are not attaching to the same area of heat sink. Since the parasitic inductance is higher than single device half bridge, 12 V/-3 V negative biased V_{gs} voltage is applied to avoid the fault turn on due to the voltage ringing induced by the common source inductance. The switching node area should not overlap with power GND or high voltage plates, because the parasitic capacitance will bring additional switching loss and also unstable oscillation. Since the high dv/dt slew rate voltage change in switching node will be coupled to the low voltage signal side through high side isolated power supply, low isolation capacitance (< 3 pF) power supply is selected and a common mode choke can effectively reduce the peak of common mode current.

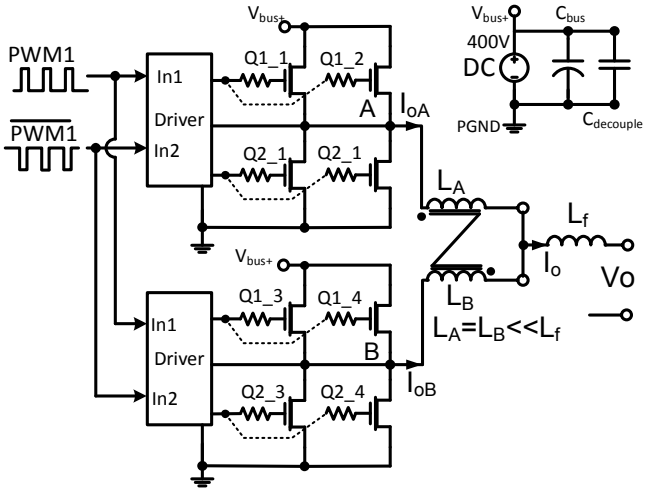
The same hard switching tests are conducted for verification. It can be seen that both high and low side devices safely and repeatedly switch to 50 A without slowing down the switching speed (R_g = 0).

B. 2N devices paralleling

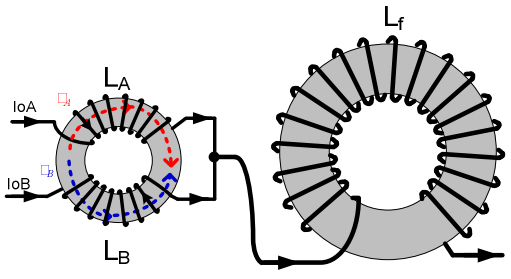
For even higher power application, more than 2 devices in parallel are required. However, the parasitic inductance and gate loop areas will further increase, and it is very hard to make the gate circuit symmetrical to each devices. Interleaving control is a good way to increase the power rating and reduce the voltage and current ripple, but the circulating current control and PWM optimization make the system complex [14-17]. For the medium power rating, paralleling device is still an attractive way. In this paper, two half bridge circuits being connected through an inversely coupled inductor is proposed, as shown in Fig. 5. The two half bridges have the same input PWM signals, and the output power rating is doubled. Inversely coupled inductor provides larger inductance so as to block the circulating current between two switching nodes. For example, $L_A = L_B = L_0$, if the coupling coefficient k of L_A and L_B is -1, the loop inductance between switching node A and B will be:

$$L_{loop} = L_A + L_B + 2L_M = 4L_0 \quad (1)$$

In this way, a very small inversely coupled inductor is applied. The coupled inductor and main inductor can be built on two separate toroid cores. In the switching test, $L_A = L_B = 7$ µH, where the coupling coefficient is -0.98, and L_f is 38 µH. Since the switching nodes are separated by the coupled inductor, two separated drivers are applied to drive the paralleling devices, respectively. Although there will be some time delay between two IC driving signals due to the different propagation time, the coupled inductor will block the high circulating current caused by the voltage difference.



(a)



(b)

Fig. 5: 4 paralleling GaN HEMTs half bridge: (a) 2 devices in parallel half-bridge circuits in Fig. 4 (a) are further paralleled by a coupled inductor; (b) Coupled inductor and main output inductor made by two toroid cores.

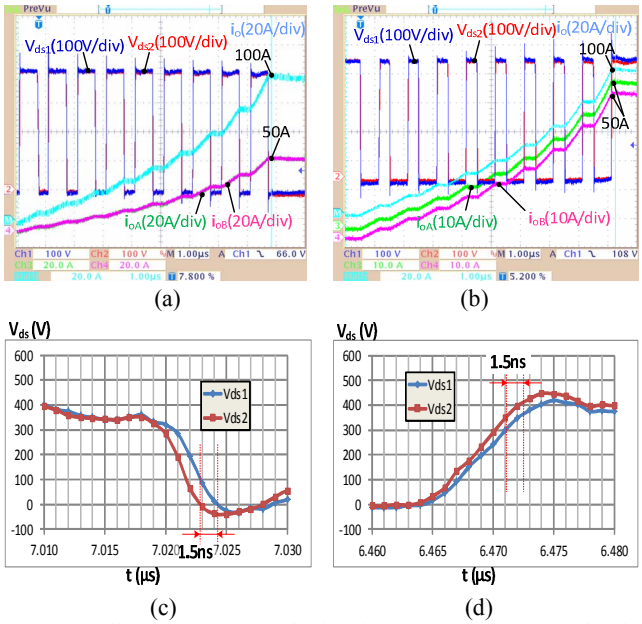


Fig. 6: 4 paralleling GaN HEMTs half bridge switching test: (a) High side hard switching to 100 A; (b) High side hard switching to 100 A; (c) Time difference of turn on time; (d) Time difference of turn off time.

Fig. 6 gives the switching test results for 4 devices paralleling half bridge. It successfully hard switches to over 100 A for both high side and low side devices. Although there must exist propagation time difference between different drivers, the current on each leg are still balanced as the loop inductor avoids circulating current. In 40 A of i_L, the propagation time of two legs has 1.5 ns difference, while it will bring huge oscillation current if these four devices are directly paralleled. For the maximum propagation time difference T_{delay}, the value coupled inductor can be calculated in equation (2) to limit the circulation current lower than I_{cir_max}:

$$L_{loop} \geq \frac{\Delta V_{ab} \cdot T_{delay}}{I_{cir\_max}} \tag{2}$$

For example, when T_{delay} is 10 ns, 1 μH L_A and L_B is enough to limit the circulating current below 1 A. When ΔV_{ab} becomes zero, the same value but opposite direction of flux $\emptyset_A$ and $\emptyset_B$ will be cancelled each other, so there is very small core loss on the coupled inductor.

By using inversely coupled inductor, it is easy to extend to 2 x N (N > 2) devices in parallel without package and PCB layout limitation. The coupled inductors can be integrated in one ferrite core with N air-gapped legs, as shown in Fig. 7. The coupling coefficient k_{ij} becomes 1/(n-1), and the loop inductance between inductor i and j is:

$$L_{loop\_ij} = L_i + L_j + 2L_{M\_ij} = \frac{2n}{n-1} L_0 \tag{3}$$

It is seen that the loop inductance is still higher than $2L_0$. All driver ICs are controlled by the same PWM signals, and it is not sensitive to the propagation time delay, so the control system is not as complex as interleaving topology.

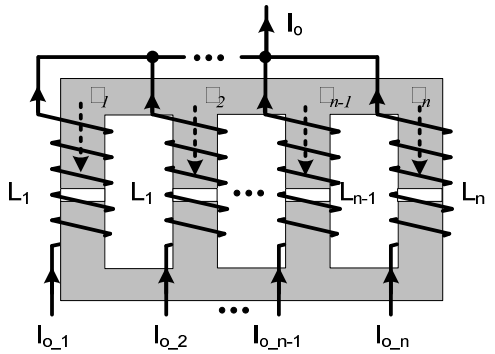


Fig. 7: Structure of n coupled inductors using n legs of ferrite core.

C. *Efficiency improvement at low power*

The power rating can be scaled up by paralleling more devices. Ideally, if the components' ratings are scaled up proportionally, the efficiency for paralleled devices will have the same optimum value but locate at a higher output power level [12]. In The same switching frequency condition, for the parallel device, the efficiency will be lower at low output power because the switching loss is dominant. In order to improve the efficiency at low power, the partial phase operation method can also be applied in this paralleling circuit [18]. Fig. 8 shows the output current waveforms during one half bridge leg is switching between on and off states. When one phase leg is off, there is only small current ripple charging and discharging the output capacitor C_{oss} of GaN HEMTs. This current will only result in small conduction loss but will not bring switching loss on the "off state" leg, so the efficiency at low power will be improved. In Fig. 8, when leg B turns "on" during the operation, the current on L_A and L_B will be balanced in a very short time. In the "off" state, leg B will see small current ripple as the GaN HEMT has only 113 pF of C_{oss} for charging/discharging, so the conduction loss is

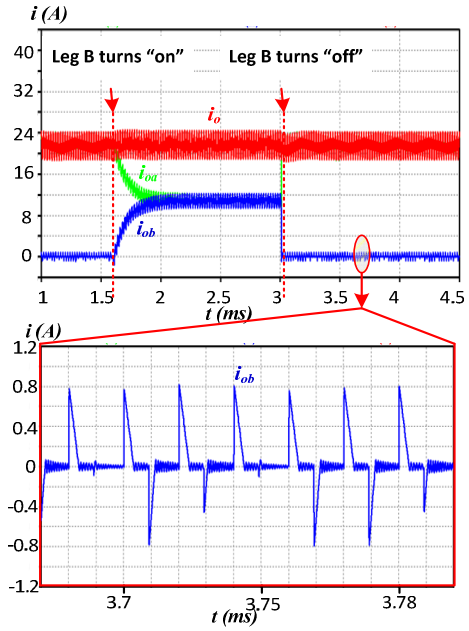


Fig. 8: Partial phase mode simulation: half bridge Leg B turns on and off at 1.6 ms and 3 ms, respectively, showing good current sharing at "on" state and low current ripple at "off" state.

very small. In order to reduce the high voltage spikes during high current transient condition, very small RC snubber circuits with 22 pF are paralleled with GaN HEMTs, and additional small switching loss in "off" state half bridge is introduced. In partial phase mode, the core loss of coupled inductor should be taken into account as the flux is not zero. However, the inductor is so small that the power loss on the inductor can be ignored.

IV. Experimental Results and Discussion

A 5 kW 2 x 2 paralleling TPH3006PS GaN HEMTs half bridge circuit is built up in the lab, as shown in Fig. 9. The GaN HEMTs are mounted on big heat sinks for high power

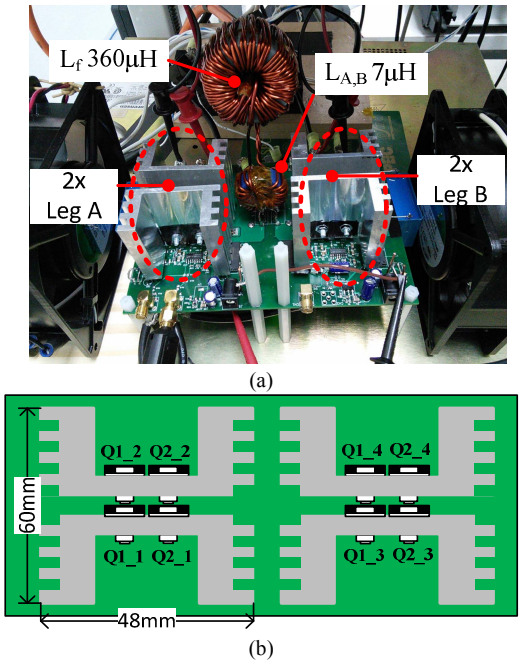


Fig. 9: 5 kW 2x2 paralling GaN HEMTs half bridge. (a) Photo of testing circuit; (b) Placement of GaN devices mounting on heatsinks.

operation. The output inductor L_f is a 360 µH/ 21 mΩ inductor made by two stacked MPP 55439A2 cores and two strands of twisted 14 AWG magnet wires. The 7 µH/5 mΩ inversely coupled inductor is made by a HS270060 core and 8 turns of 14 AWG magnet wire. The half bridge circuit is configured to work in 200 V input/ 400 V output synchronous boost converter mode to evaluate the performance. 50% fixed duty cycle of complementary PWM signals inserted by 100 ns dead time with different switching frequencies are applied to the input of drivers.

The efficiency test is firstly conducted on 2x paralleling half bridge Leg A. In this condition, the inversely coupled inductor is removed and only an 860 µH/48 mΩ inductor made by one MPP core 55192A2 and 14 AWG magnet wire is employed. It can be seen in Fig. 10, the peak efficiency is 99.15% at 1.05 kW for 50 kHz f_{sw}, and 98.8% at similar power rating for 100 kHz f_{sw}. For the 4x paralleling test, the peak efficiency is 99.11% and 98.79% for 50 kHz and 100 kHz,

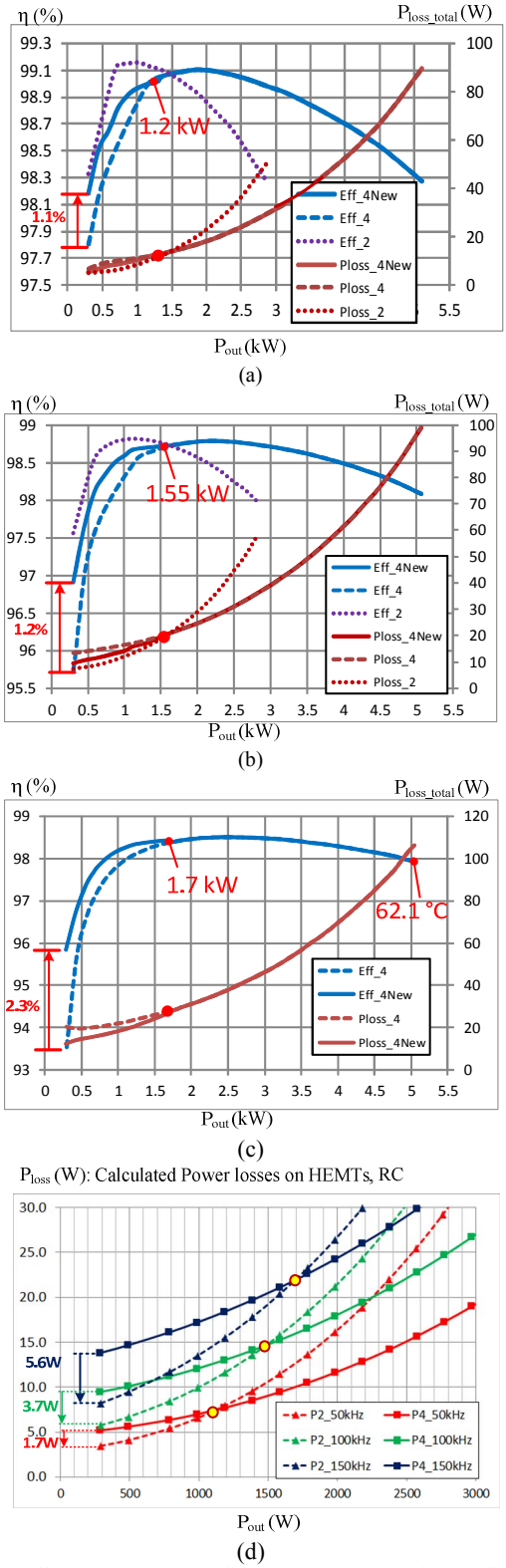
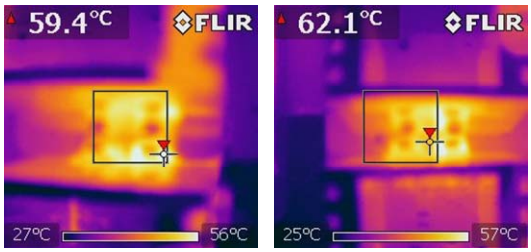


Fig. 10: Efficiency test in synchronous boost mode for 2x directly paralleling and 4x paralleling through inversely coupled inductor. (a) f_{sw} = 50 kHz; (c) f_{sw} = 100 kHz. (c) f_{sw} = 150 kHz; (d) At low output power, 2x paralleling shows lower power loss, and the switching loss contributes more with the switching frequency increasing, partial phase method can be applied.

respectively. The coupled inductor brings about 0.5 W additional losses at peak efficiency point.

At the low power, the partial phase mode can be applied to improve the efficiency further. The efficiency at 300W can be improved by 1.1%, 1.2% and 2.3% in the switching frequency at 50 kHz, 100 kHz, and 150 kHz, respectively. This method is more helpful for higher switching frequency as the switching loss contributes more percentage to the total loss.

Each pair of high side and low side half bridge devices are mounted on a heat sink with 2.2 °C/W in the condition of 5m/s air flow. It is easy to run at 5 kW output power, while the temperature rising is less than 40 °C. As shown in Fig. 11, the case temperatures of each leg are only 59.4 °C and 62.1 °C. The reason for temperature difference is that there are 0.4 m/s air flow speed bias (5.4 m/s for Leg A, 5 m/s for Leg B). Even higher power rating can be expected as the enough temperature rising room allows extra 60 W power losses on the devices.



Leg A Leg B

Fig. 11: Temperature measurement of Leg A and Leg B at P_o = 5150 W, f_{sw} = 150 kHz, and ambient temperature T_a = 24 °C.

By using higher current rating discrete GaN HEMTs in parallel, such as 60 mΩ TO247 device, the power level of a full bridge converter can be extended to tens of kW. In the meantime, interleaving method for high power PFC and inverters can also be applied for better system performance.

V. CONCLUSION

In this paper, the driver circuit and layout design for leaded packaged GaN HEMTs in parallel are discussed. A half bridge circuit combined with paralleling directly and by coupled inductor is designed and demonstrated. Both high side and low side devices are composed of four GaN HEMTs (600 V/17 A) in parallel, respectively. Multi-pulse switching test results show both high side and low side devices of The efficiency test in 200 V input / 400 V output synchronous boost mode is showing that the output power can be scaled up to 5 kW while there is still enough room for higher output power. It achieves efficiency as high as 99.1% at 50 kHz. In this way, there is no limitation for paralleling more GaN HEMTs to achieve higher power rating. Partial phase method is also applied, and the efficiency is further improved at low power level, especially for higher switching frequency.

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