TPH3205WSBQA

Not recommended for new designs—see TP65H050WSQA

AEC-Q101 Qualified 650V GaN FET in TO-247 (source tab)

Description

The TPH3205WSBQA 650V, 49mΩ Gallium Nitride (GaN) FET is a normally-off automotive (AEC-Q101) qualified device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

Transphorm GaN offers improved efficiency over silicon, through lower gate charge, lower crossover loss, and smaller reverse recovery charge.

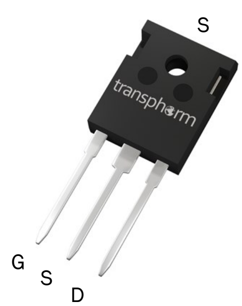
Related Literature

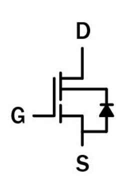
- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing
- AN0010: Paralleling GaN FETs

Ordering Information

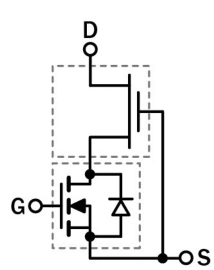
Part Number	Package	Package Configuration
TPH3205WSBQA	3 lead TO-247	Source

TPH3205WSBQA
TO-247
(top view)





Cascode Schematic Symbol



Cascode Device Structure

Features

- JEDEC and AEC-Q101 qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - Intrinsic lifetime tests
  - Wide gate safety margin
  - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Automotive
- Datacom
- Broad industrial
- PV inverter
- Servo motor

Key Specifications	
V_{DSS} (V)	650
$V_{(TR)DSS}$ (V)	800
$R_{DS(on)eff}$ (mΩ) max*	62
Q_{RR} (nC) typ	136
Q_G (nC) typ	28

* Dynamic on-resistance; see Figures 19 and 20

Common Topology Power Recommendations	
CCM bridgeless totem-pole*	2983W max
Hard-switched inverter**	3581W max

Conditions: F_{SW}=45kHz; T_J=115°C; $T_{HEATSINK}$=90°C; insulator between device and heatsink (6 mil Sil-Pad® K-10); power de-rates at lower voltages with constant current

* V_{IN}=230V_{AC}; V_{OUT}=390V_{DC}
** V_{IN}=380V_{DC}; V_{OUT}=240V_{AC}

Absolute Maximum Ratings (T_c=25°C unless otherwise stated.)

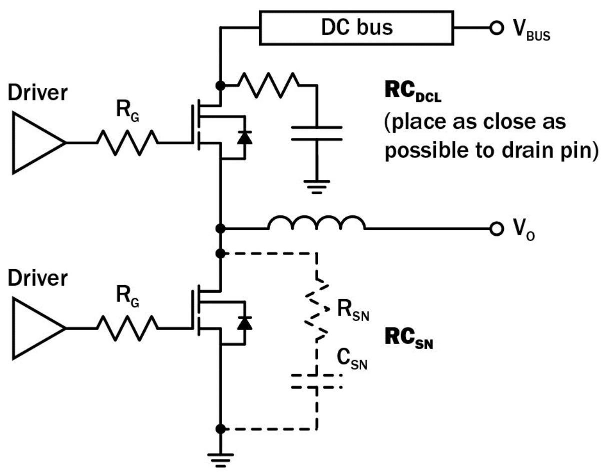
Symbol	Parameter		Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
$V_{(TR)DSS}$	Transient drain to source voltage [a]		800	
V_{GSS}	Gate to source voltage		±18	
P_D	Maximum power dissipation @T_C=25°C		125	W
I_D	Continuous drain current @T_C=25°C [b]		35	A
	Continuous drain current @T_C=100°C [b]		22	A
I_{DM}	Pulsed drain current (pulse width: 10µs)		150	A
$(di/dt)_{RDMC}$	Reverse diode di/dt, repetitive [c]		1500	A/µs
$(di/dt)_{RDMT}$	Reverse diode di/dt, transient [d]		2900	A/µs
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{SOLD}	Soldering peak temperature [e]		260	°C

Notes:
a. In off-state, spike duty cycle D<0.01, spike duration <1µs
b. For increased stability at high current operation, see Circuit Implementation on page 3
c. Continuous switching operation
d. ≤300 pulses per second for a total duration ≤20 minutes
e. For 10 sec., 1.6mm from the case

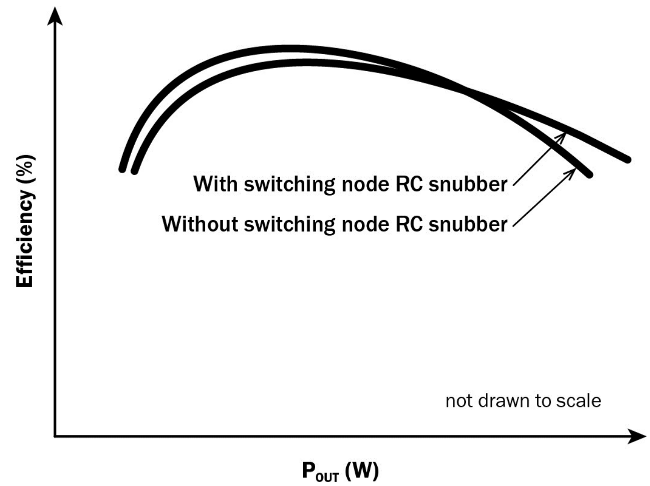
Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	1	°C/W
$R_{\Theta JA}$	Junction-to-ambient	40	°C/W

Circuit Implementation



Simplified Half-bridge Schematic



Efficiency vs Output Power

Recommended gate drive: (0V, 8-10V) with $R_{G(tot)}$ = 15Ω, where $R_{G(tot)} = R_G + R_{DRIVER}$

Required DC Link RC Snubber (RC_{DCL}) [a]	Recommended Switching Node RC Snubber (RC_{SN}) [b, c]
[10nF + 8Ω] x 2	100pF + 10Ω

Notes:

a. RC_{DCL} should be placed as close as possible to the drain pin

b. A switching node RC snubber (C, R) is recommended for high switching currents (>70% of I_{RDMC1} or I_{RDMC2}; see page 5 for I_{RDMC1} and I_{RDMC2})

c. I_{RDM} values can be increased by increasing R_G and C_{SN}

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	1.6	2.1	2.6	V	$V_{DS}=V_{GS}$, I_D=0.7mA
$R_{DS(on)eff}$	Drain-source on-resistance [a]	—	49	62	mΩ	V_{GS}=8V, I_D=22A
		—	105	—		V_{GS}=8V, I_D=22A, T_J=150°C
I_{DSS}	Drain-to-source leakage current	—	4	40	μA	V_{DS}=650V, V_{GS}=0V
		—	50	—		V_{DS}=650V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=18V
	Gate-to-source reverse leakage current	—	—	-100		V_{GS}=-18V
C_{ISS}	Input capacitance	—	2200	—	pF	V_{GS}=0V, V_{DS}=400V, *f*=1MHz
C_{OSS}	Output capacitance	—	135	—		
C_{RSS}	Reverse transfer capacitance	—	23	—		
$C_{O(er)}$	Output capacitance, energy related [b]	—	190	—	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related [c]	—	300	—		
Q_G	Total gate charge	—	28	42	nC	V_{DS}=400V, V_{GS}=0V to 8V, I_D=22A
Q_{GS}	Gate-source charge	—	10	—		
Q_{GD}	Gate-drain charge	—	6	—		
Q_{OSS}	Output charge	—	107.4	—	nC	V_{GS}=0V, V_{DS}=0V to 400V
$t_{D(on)}$	Turn-on delay	—	36	—	ns	V_{DS}=400V, V_{GS}=0V to 8V, I_D=22A, R_G=10Ω
t_R	Rise time	—	7.6	—		
$t_{D(off)}$	Turn-off delay	—	40	—		
t_F	Fall time	—	8.6	—		

Notes:
a. Dynamic on-resistance; see Figures 19 and 20 for test circuit and conditions
b. Equivalent capacitance to give same stored energy as V_{DS} rises from 0V to 400V
c. Equivalent capacitance to give same charging time as V_{DS} rises from 0V to 400V

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	22	A	V_{GS}=0V, T_C=100°C, ≤25% duty cycle
V_{SD}	Reverse voltage [a]	—	2.0	2.4	V	V_{GS}=0V, I_S=22A
		—	1.5	1.7		V_{GS}=0V, I_S=11A
t_{RR}	Reverse recovery time	—	40	—	ns	I_S=22A, V_{DD}=400V, di/dt=1000A/µs
Q_{RR}	Reverse recovery charge	—	136	—	nC	
$(di/dt)_{RDMC}$	Reverse diode di/dt, repetitive [b]	—	—	1500	A/µs	
I_{RDMC1}	Reverse diode switching current, repetitive (dc) [c, e]	—	—	23	A	Circuit implementation and parameters on page 3
I_{RDMC2}	Reverse diode switching current, repetitive (ac) [c, e]	—	—	27	A	Circuit implementation and parameters on page 3
$(di/dt)_{RDMT}$	Reverse diode di/dt, transient [d]	—	—	2900	A/µs	
I_{RDMT}	Reverse diode switching current, transient [d,e]	—	—	35	A	Circuit implementation and parameters on page 3

Notes:
a. Includes dynamic $R_{DS(on)}$ effect
b. Continuous switching operation
c. Definitions: dc = dc-to-dc converter topologies; ac = inverter and PFC topologies, 50-60Hz line frequency
d. ≤300 pulses per second for a total duration ≤20 minutes
e. I_{RDM} values can be increased by increasing R_G and C_{SN} on page 3

Typical Characteristics (T_C=25°C unless otherwise stated)

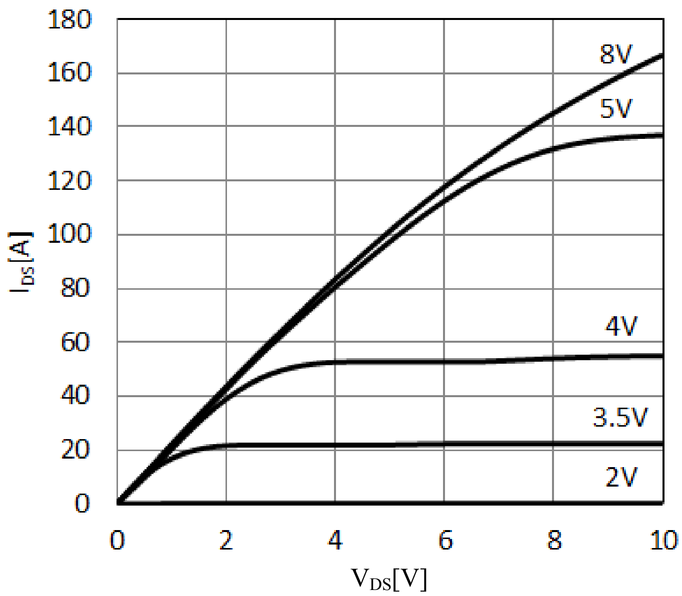


Figure 1. Typical Output Characteristics T_J=25°C
Parameter: V_{GS}

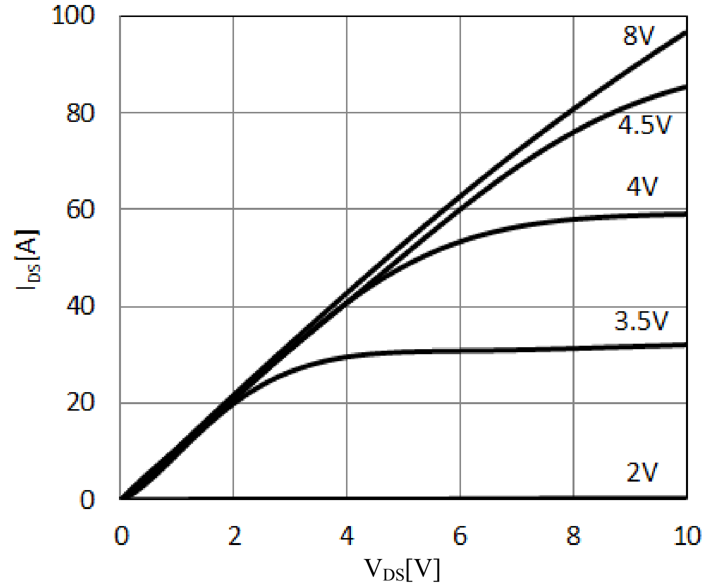


Figure 2. Typical Output Characteristics T_J=150°C
Parameter: V_{GS}

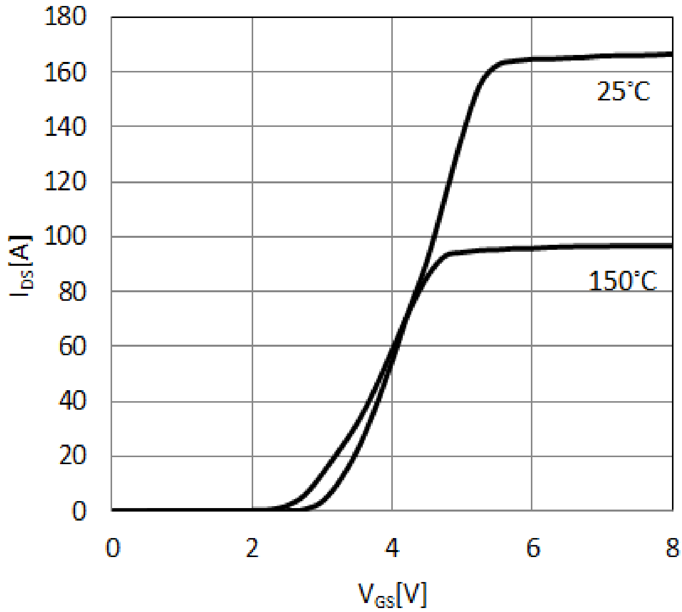


Figure 3. Typical Transfer Characteristics
V_{DS}=10V, parameter: T_J

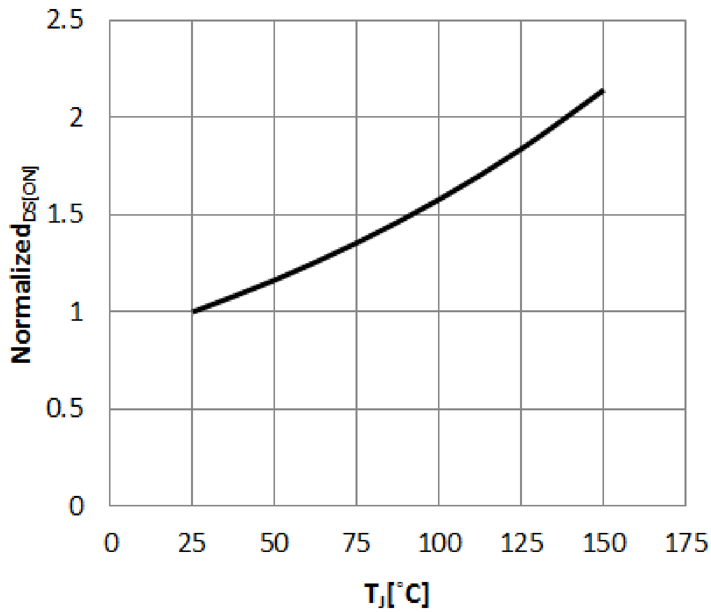


Figure 4. Normalized On-resistance
I_D=22A, V_{GS}=8V

Typical Characteristics (T_C=25 °C unless otherwise stated)

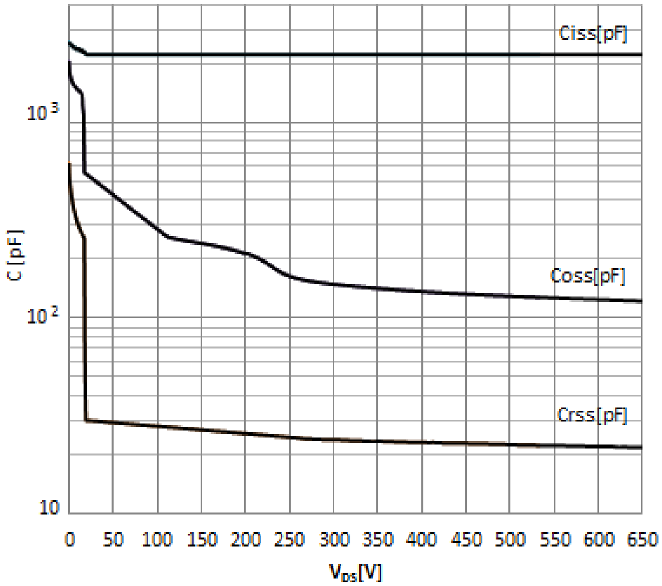


Figure 5. Typical Capacitance
V_{GS}=0V, f=1MHz

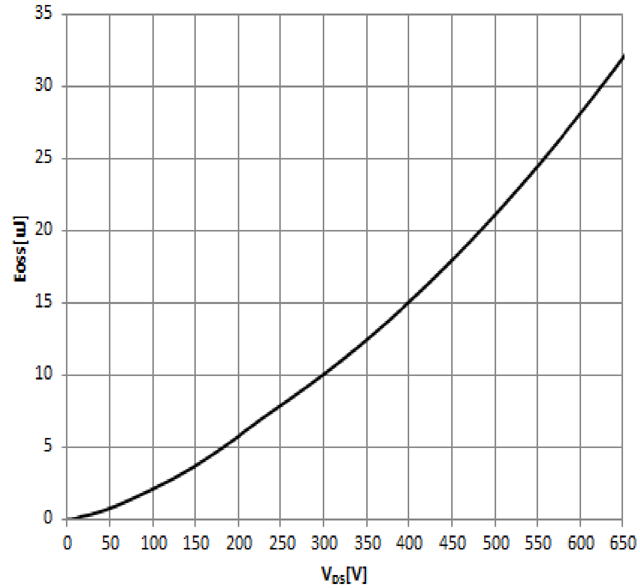


Figure 6. Typical C_{OSS} Stored Energy

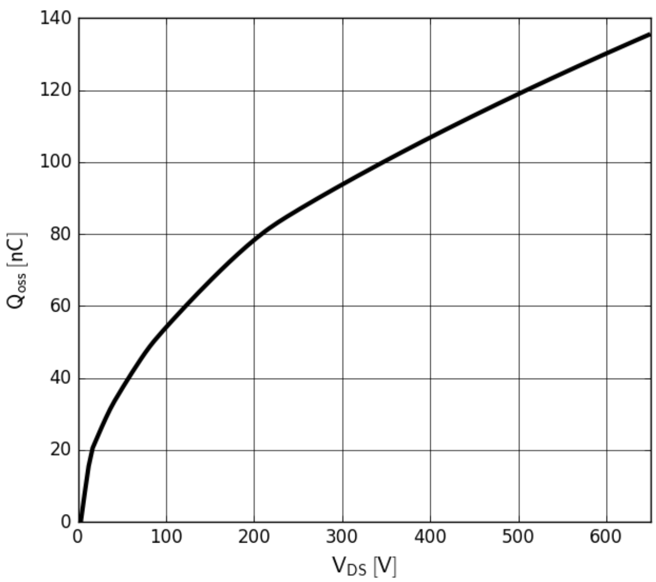


Figure 7. Typical Q_{OSS}

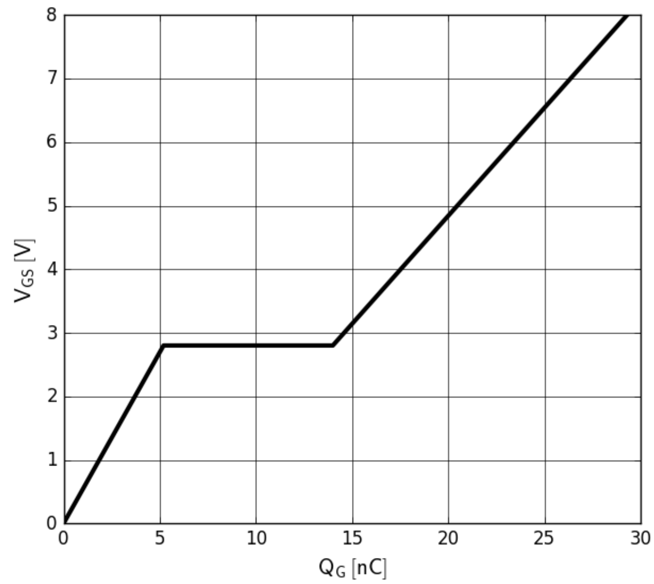


Figure 8. Typical Gate Charge
I_{DS}=22A, V_{DS}=400V

Typical Characteristics (T_C=25 °C unless otherwise stated)

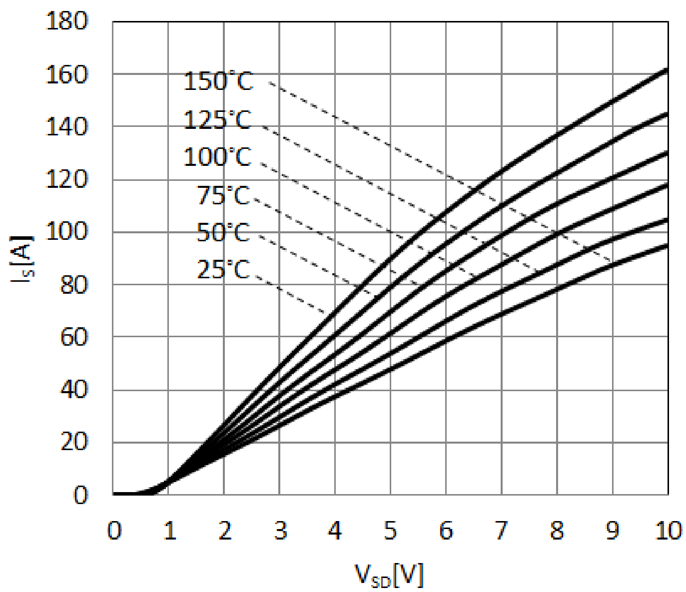


Figure 9. Forward Characteristics of Rev. Diode
I_S=f(V_{SD}); parameter: T_J; pulse width = 20μs

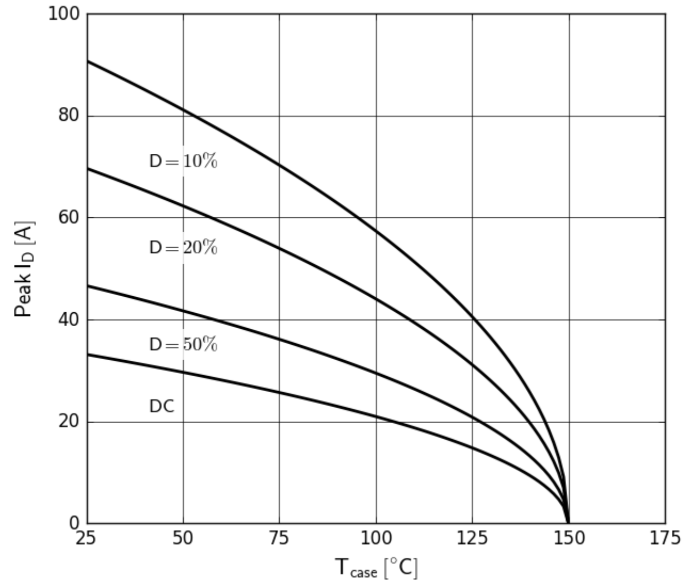


Figure 10. Current Derating
Pulse width ≤ 10μs

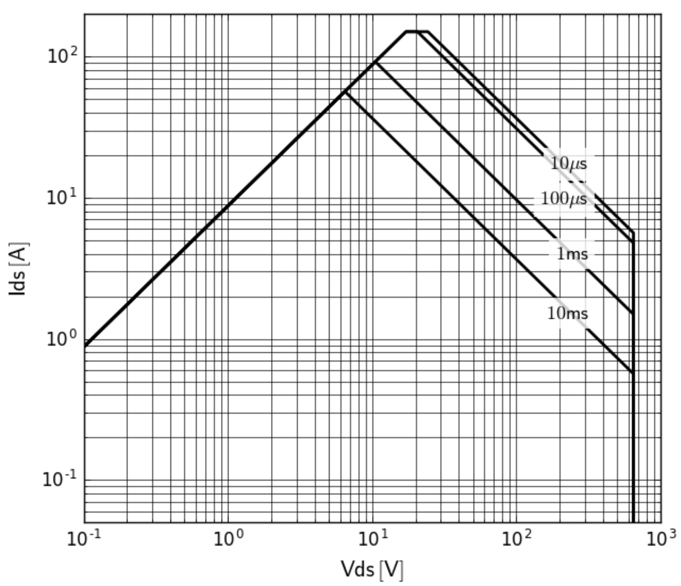


Figure 11. Safe Operating Area T_C=25 °C
(calculated based on thermal limit)

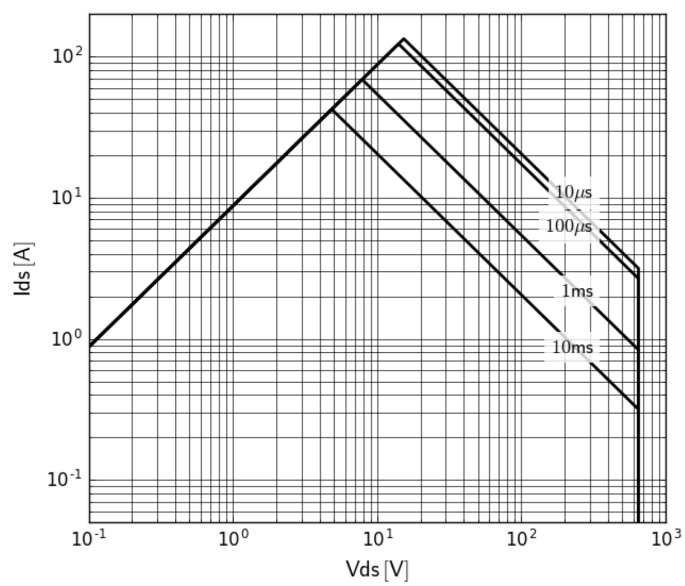


Figure 12. Safe Operating Area T_C=80 °C
(calculated based on thermal limit)

Typical Characteristics (T_C=25 °C unless otherwise stated)

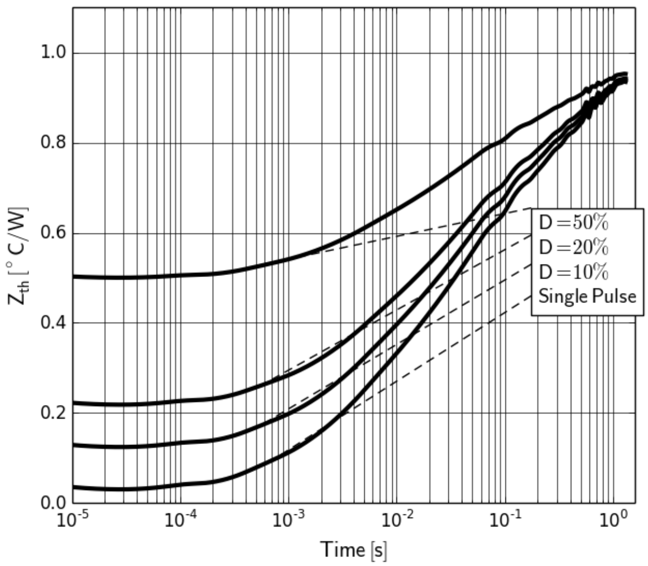


Figure 13. Transient Thermal Resistance

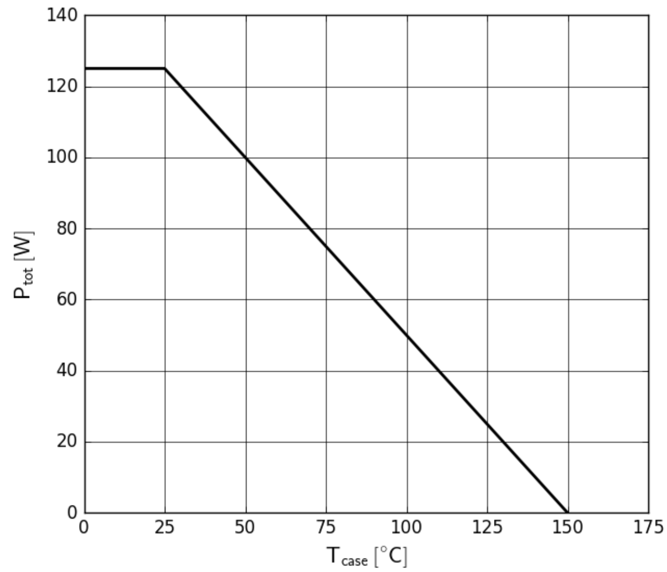


Figure 14. Power Dissipation

Test Circuits and Waveforms

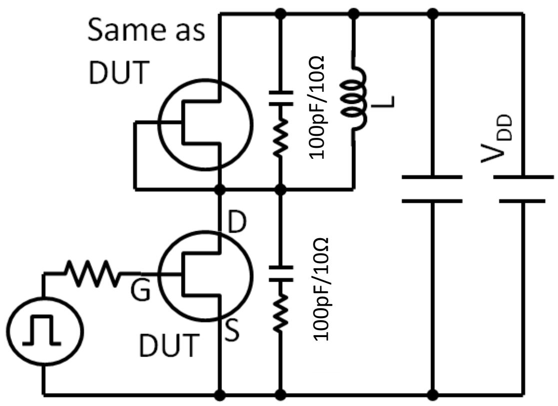


Figure 15. Switching Time Test Circuit
(see circuit implementation on page 3
for methods to ensure clean switching)

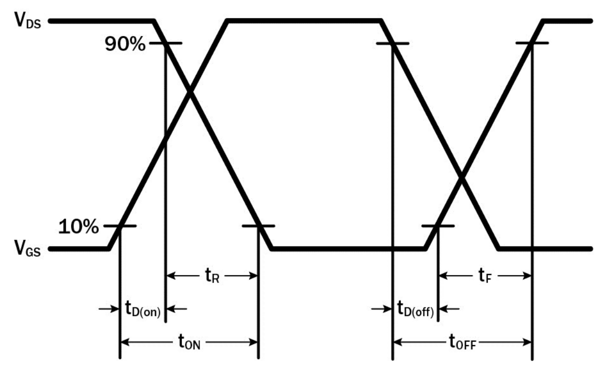


Figure 16. Switching Time Waveform

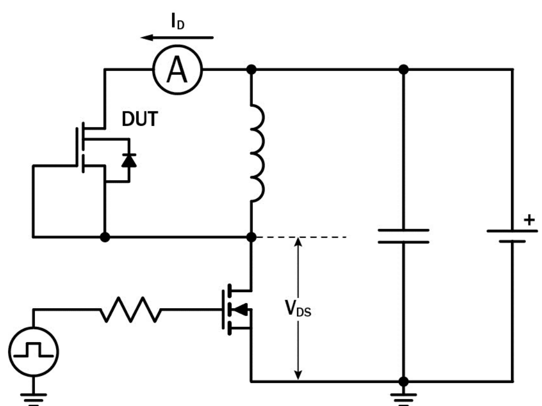


Figure 17. Diode Characteristics Test Circuit

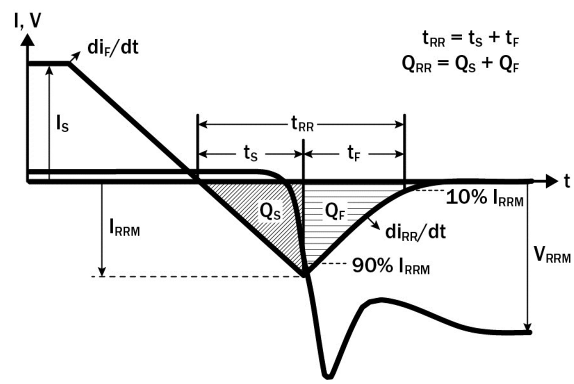


Figure 18. Diode Recovery Waveform

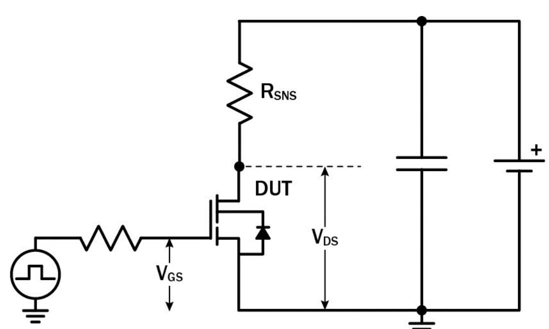
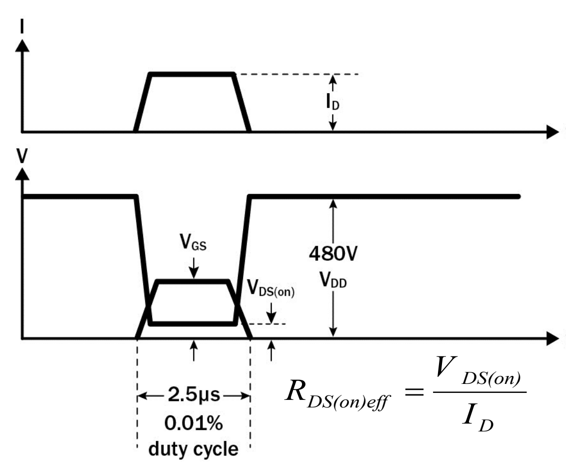


Figure 19. Dynamic $R_{DS(on)eff}$ Test Circuit



$$R_{DS(on)eff} = \frac{V_{DS(on)}}{I_D}$$

Figure 20. Dynamic $R_{DS(on)eff}$ Waveform

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

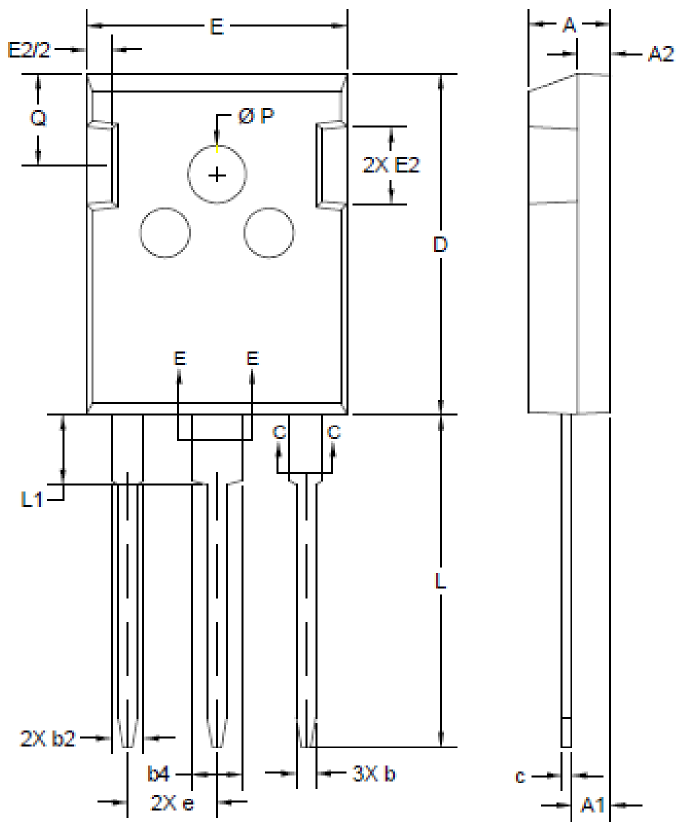
GaN Design Resources

The complete technical library of GaN design tools can be found at transphormusa.com/design:

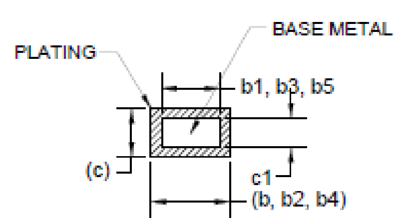
- Reference designs
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Mechanical

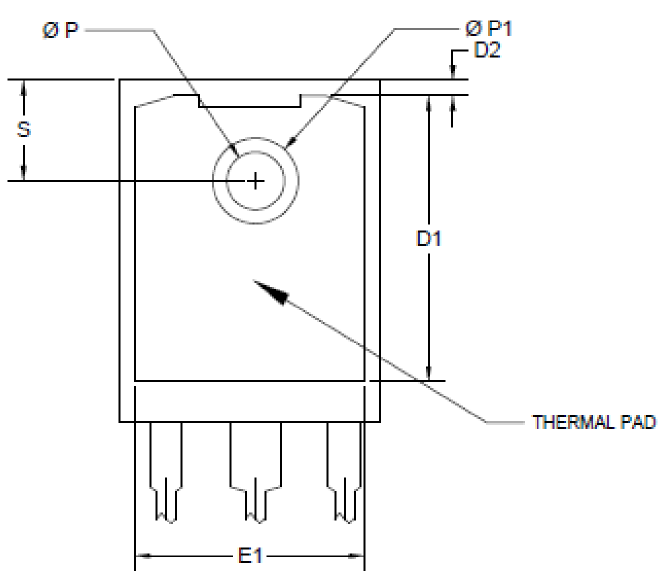
3 Lead TO-247 Package



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.82	5.00	5.19	0.190	0.197	0.204
A1	2.20	2.39	2.57	0.087	0.094	0.101
A2	1.82	2.01	2.18	0.072	0.079	0.086
b	1.09	1.19	1.35	0.043	0.047	0.053
b1	1.09	-	1.30	0.043	-	0.051
b2	1.87	2.03	2.31	0.074	0.080	0.091
b3	1.87	-	2.27	0.074	-	0.089
b4	2.94	3.05	3.22	0.116	0.120	0.127
b5	2.94	-	3.18	0.116	-	0.125
c	0.50	0.58	0.68	0.020	0.023	0.027
c1	0.50	-	0.64	0.020	-	0.025
D	20.67	20.85	21.11	0.814	0.821	0.831
D1	17.20	-	17.63	0.677	-	0.694
D2	0.81	-	1.20	0.032	-	0.048
E	15.72	15.90	16.15	0.619	0.626	0.636
E1	13.79	-	14.25	0.543	-	0.561
E2	4.30	-	4.86	0.169	-	0.191
e	5.46 BSC			0.215 BSC		
L	19.55	19.94	20.38	0.770	0.785	0.802
L1	3.93	4.11	4.48	0.155	0.162	0.176
ØP	3.50	3.61	3.69	0.138	0.142	0.145
ØP1	7.08	7.19	7.32	0.279	0.283	0.288
Q	5.41	-	5.85	0.213	-	0.230
S	6.15 BSC			0.242 BSC		



SECTION C-C, E-E



NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS D1 & E1.
3. LEAD FINISH UNCONTROLLED IN L1.
4. OUTLINE CONFORMS TO JEDEC TO-247AD.

TO-247 3L			
transphorm			
SCALE: 1:1	SHEET 1/1	DRAWING NO. 200019	VER. 3

Revision History

Version	Date	Change(s)
0	3/1/2017	QA version denotes AEC-Q101 qualification
1	11/1/2017	**Updated** effective on-resistance symbol to $R_{DS(on)eff}$ to adhere to new JEDEC standards; **Added** common topology max power recommendations (pg 1), switching current values (pg 2), Circuit Implementation (pg 3), Q_{OSS} value (pg 4), Figures 7 & 8 (pg 6)
2	10/31/2019	marked NRND—see TP65H050WSQA