

900V Cascode GaN FET in TO-247

Not Recommended for New Design

Description

The TP90H050WS 900V, 50m Ω Gallium Nitride (GaN) FET is a normally-off device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

Transphorm GaN offers improved efficiency over silicon, through lower gate charge, lower crossover loss, and smaller reverse recovery charge.

Related Literature

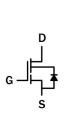
- ANOOO9: Recommended External Circuitry for GaN FETs
- ANOOO3: Printed Circuit Board Layout and Probing
- ANOO10: Paralleling GaN FETs

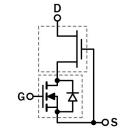
Ordering Information

Part Number	Package	Package Configuration	
TP90H050WS	3 lead TO-247	Source	

TP90H050WS T0-247 (top view)







Cascode Schematic Symbol

Cascode Device Structure

Features

- JEDEC qualified GaN technology
- Dynamic R_{DS(on)eff} production tested
- · Robust design, defined by
 - Intrinsic lifetime tests
 - Wide gate safety margin
 - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- · RoHS compliant and Halogen-free packaging

Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
 - Increased power density
 - Reduced system size and weight
 - Overall lower system cost
- Achieves increased efficiency in both hard- and softswitched circuits
- Easy to drive with commonly-used gate drivers
- · GSD pin layout improves high speed design

Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor

Key Specifications		
V _{DS} (V)	900	
V _{(TR)DSS} (V) max	1000	
$R_{DS(on)eff}(m\Omega)\;max^*$	63	
Q _{RR} (nC) typ	156	
Q _G (nC) typ	15	

^{*} Reflects both static and dynamic on-resistance; see Figures 18 and 19

Absolute Maximum Ratings (T_J =25 °C unless otherwise stated. All recommended current levels (I_{DM}) are based on adequate heat sinking, ensuring T_J =150 °C)

Symbol	Parameter		Limit Value	Unit
	Continuous drain current @T _C =25°C a		34	А
l _D	Continuous drain current @T _C =	Continuous drain current @T _C =100°C a		А
I _{DM}	Pulsed drain current (pulse wi	dth: 10µs)	150	А
di/dt _{RDMC}	Reverse diode di/dt, repetitive	b p	1600	A/µs
I _{RDMC1}	Reverse diode switching curre	nt, repetitive (dc) c	24	Α
I _{RDMC2}	Reverse diode switching current, repetitive (ac) °		28	Α
di/dt _{RDMT}	Reverse diode di/dt, transient d		3000	A/µs
I _{RDMT}	Reverse diode switching current, transient		36	А
V _{(TR)DSS}	Transient drain to source voltage e		1000	V
V _{GSS}	Gate to source voltage		±20	V
P _D	Maximum power dissipation @T _C =25°C		119	W
Tc	Operating temperature	Case	-55 to +150	°C
TJ	Operating temperature	Junction	-55 to +150	°C
Ts	Storage temperature		-55 to +150	°C
T _{SOLD}	Soldering peak temperature ^f Mounting Torque		260	°C
-			80	N cm

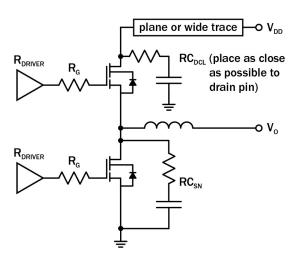
Notes:

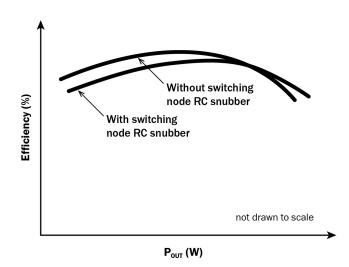
- a. For increased stability at high current operation, see Circuit Implementation on page 3
- b. Continuous switching operation
- c. Definitions: dc = dc to dc converter topologies; ac = inverter and PFC topologies, 50-60Hz line frequency
- d. ≤300 pulses in 1 second
- e. In off-state, spike duty cycle D<0.01, spike duration $<1\mu$ s
- f. For 10 sec., 1.6mm from the case

Thermal Resistance

Symbol	Parameter	Typical	Unit
Rejc	Junction-to-case	1.05	°C/W
Roja	Junction-to-ambient	40	°C/W

Circuit Implementation





Simplified Half-bridge Schematic

Efficiency vs Output Power

Recommended gate drive: (0V, 12-14V) with $R_{G(tot)}$ = 22-30 Ω , where $R_{G(tot)}$ = R_G + R_{DRIVER}

Required DC Link RC Snubber (RC _{DCL}) ^a	Recommended Switching Node RC Snubber (RCsN) b		
[10nF + 8Ω] x 2	100pF + 10Ω		

Notes:

- a. RC_DCL should be placed as close as possible to the drain pin
- b. A switching node RC snubber (C, R) is recommended for high switching currents (>70% of IRDMC1 or IRDMC2)

Electrical Parameters (T_J=25 °C unless otherwise stated)

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
Forward D	Device Characteristics				1	
V _{(BL)DSS}	Maximum drain-source voltage	900	_	_	V	V _{GS} =0V
V _{GS(th)}	Gate threshold voltage	3.4	3.9	4.4	V	V _{DS} =V _{GS} , I _D =0.7mA
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	_	-6.5	_	mV/°C	
В	Drain-source on-resistance ^a	_	50	63	mΩ	V _{GS} =10V, I _D =22A
R _{DS(on)eff}		_	105	_		V _{GS} =10V, I _D =22A, T _J =150°C
l		_	4	40	- μΑ	V _{DS} =900V, V _{GS} =0V
I _{DSS}	Drain-to-source leakage current	_	15	_		V _{DS} =900V, V _{GS} =0V, T _J =150°C
	Gate-to-source forward leakage current	_	_	100	4	V _{GS} =20V
I _{GSS}	Gate-to-source reverse leakage current	_	_	-100	nA	V _{GS} =-20V
C _{ISS}	Input capacitance	_	1000	_		V _{GS} =0V, V _{DS} =600V, <i>f</i> =1MHz
Coss	Output capacitance	_	115	_	pF	
Crss	Reverse transfer capacitance	_	3.5	_		
C _{O(er)}	Output capacitance, energy related b	_	153	_	, F	V _{GS} =0V, V _{DS} =0V to 600V
$C_{O(tr)}$	Output capacitance, time related °	_	260	_	pF	
Q _G	Total gate charge	_	15	_		V _{DS} =600V, V _{GS} =10V, I _D =22A
Q _{GS}	Gate-source charge	_	5	_	nC	
Q_{GD}	Gate-drain charge	_	4.7	_		
Qoss	Output charge	_	155	_	nC	V _{GS} =0V, V _{DS} =0V to 600V
t _{D(on)}	Turn-on delay	_	48	_		
t _R	Rise time	_	12	_		V_{DS} =600V, V_{GS} =10V, I_{D} =22A R_{G} =25 Ω , 4A driver
t _{D(off)}	Turn-off delay	_	70	_	ns	
t _F	Fall time	_	12	_		
Reverse D	Device Characteristics				ı	
Is	Reverse current	_	_	22	А	V _{GS} =0V, T _C =100°C, ≤25% duty cycle
Von	Reverse voltage ^a	_	2.2	2.6	V	V _{GS} =0V, I _S =22A
V _{SD}		_	1.6	1.9		V _{GS} =0V, I _S =11A
t _{RR}	Reverse recovery time	_	53	_	ns	I _S =22A, V _{DD} =600V,
Q _{RR}	Reverse recovery charge	_	156	_	nC	di/dt=1000A/µs

Notes:

- a. Reflects both static and dynamic on-resistance; dynamic on-resistance test setup and waveform; see Figures 18 and 19 for conditions
- b. Equivalent capacitance to give same stored energy from OV to 600V
- c. Equivalent capacitance to give same charging time from 0V to 600V

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Typical Characteristics (T_C=25 °C unless otherwise stated)

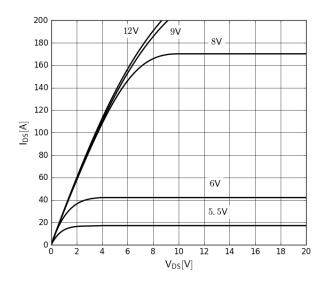


Figure 1. Typical Output Characteristics T_J=25 °C

Parameter: V_{GS}

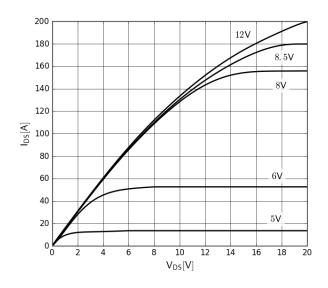


Figure 2. Typical Output Characteristics T_J=150 °C

Parameter: V_{GS}

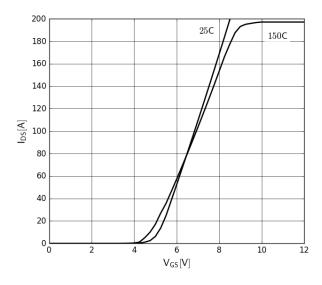


Figure 3. Typical Transfer Characteristics V_{DS} =20V, parameter: T_J

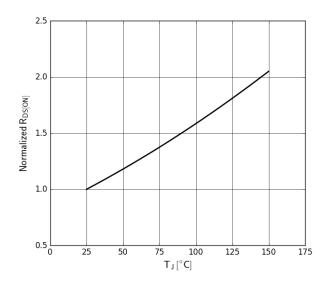


Figure 4. Normalized On-resistance $I_D=22A, V_{GS}=8V$

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Typical Characteristics (T_C=25 °C unless otherwise stated)

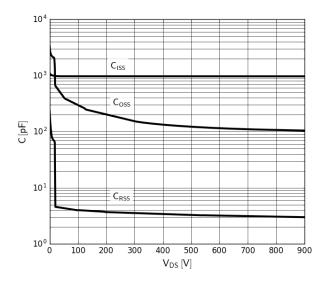


Figure 5. Typical Capacitance V_{GS} =0V, f=1MHz

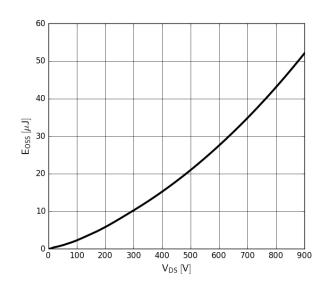


Figure 6. Typical Coss Stored Energy

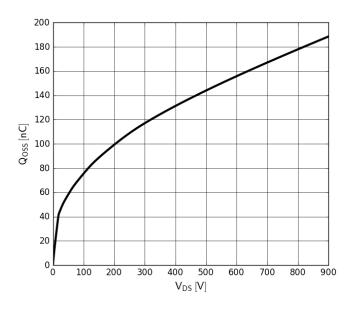


Figure 7. Typical Qoss

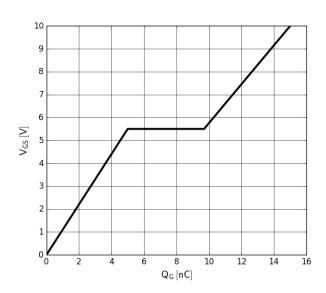


Figure 8. Typical Gate Charge I_{DS}=22A, V_{DS}=600V

Typical Characteristics (T_C=25 °C unless otherwise stated)

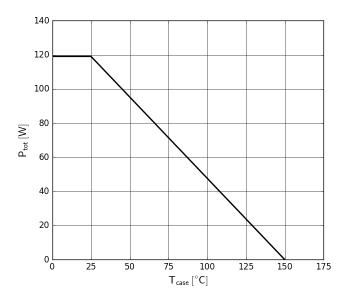


Figure 9. Power Dissipation

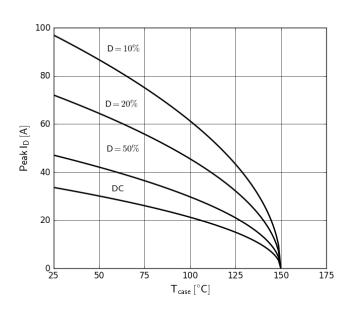


Figure 10. Current Derating Pulse width \leq 10µs, $V_{GS} \geq$ 10V

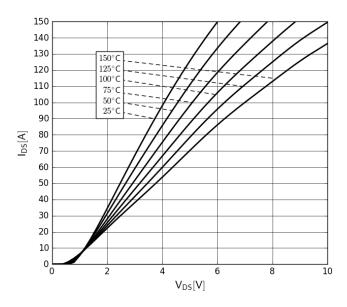


Figure 11. Forward Characteristics of Rev. Diode $I_S {=} f(V_{SD}), \ parameter; \ T_J$

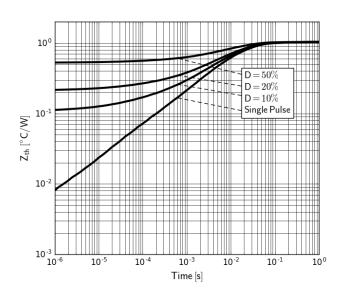


Figure 12. Transient Thermal Resistance

Typical Characteristics (T_C =25 $^{\circ}$ C unless otherwise stated)

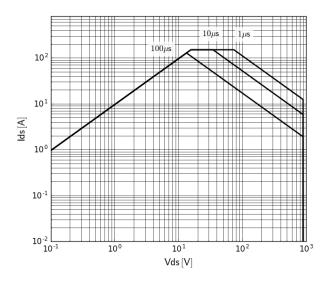


Figure 13. Safe Operating Area T_C=25°C

Test Circuits and Waveforms

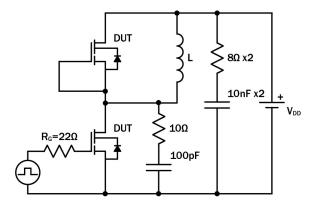


Figure 14. Switching Time Test Circuit (see Circuit Implementation on page 3 for methods to ensure clean switching)

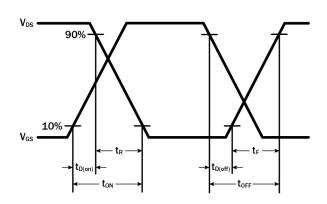


Figure 15. Switching Time Waveform

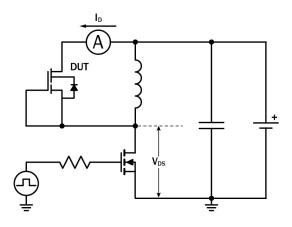


Figure 16. Diode Characteristics Test Circuit

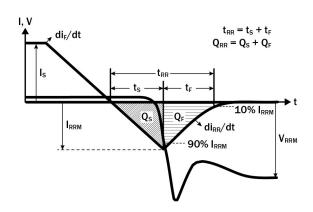


Figure 17. Diode Recovery Waveform

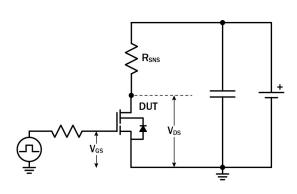


Figure 18. Dynamic R_{DS(on)eff} Test Circuit

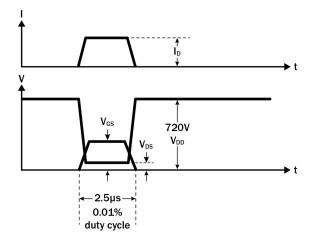


Figure 19. Dynamic R_{DS(on)eff} Waveform

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note <u>Printed Circuit Board Layout and Probing for GaN Power Switches</u>. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See ANOOO3: Printed Circuit Board Layout and Probing	

GaN Design Resources

The complete technical library of GaN design tools can be found at transphormusa.com/design:

- Evaluation kits
- Application notes
- · Design guides
- · Simulation models
- Technical papers and presentations

Mechanical

3 Lead TO-247 Package

