Short-Circuit Protection for GaN Power Devices with Integrated Current Limiter and Commercial Gate Driver

Davide Bisi*, Long Nguyen‡, Philip Zuk*, Ashish Gokhale‡, Keith Coffey‡, Ted Liu‡, Bill Cruse*,
Tsutomu Hosoda†, Masamichi Kamiyama†, Primit Parikh*, Umesh Mishra*

* Transphorm, Inc., 75 Castilian Dr., Goleta, CA 93117, USA. Corresponding Author: dbisi@transphormusa.com

† Transphorm Japan Inc., 2-5-15 Shin-Yokohama, Kouhoku-ku, Yokohama, Japan

‡ Skyworks, 200 W Cesar Chavez, Austin, TX 78701, USA

***Abstract*—A successful short-circuit protection technology for GaN power devices paired with a commercial gate driver is demonstrated. The GaN power devices have an integrated Short-Circuit Current Limiter (SCCL) to achieve a sufficiently long short-circuit withstanding time (SCWT). The SCWT is tuned from 0.3 µs to 2 µs (a remarkable 7x increase) with a relatively small penalty in on-resistance. The gate-driver has desaturation detection (DESAT) and soft shutdown circuitry to achieve a fast protection response of 800 ns with high noise immunity greater than 100 V/ns. The combination of GaN power devices with SCCL and a commercial gate driver with fast DESAT and high noise immunity allows short-circuit protection and fail-safe operation of GaN power electronics for additional robustness in motor drive applications.**

Keywords—GaN, HEMT, Power Device, Short-Circuit, SCWT, Current Limiter, SCCL, Motor Drive, Inverter, Protection Circuit, DESAT, Gate Driver

I. Introduction

High-efficiency GaN power devices are penetrating several power electronics markets, including adapters, power supply units, photovoltaic inverters, battery chargers, and motor drives. Short-circuit protection is an important requirement, especially in motor drives, where power devices may be required to survive short-circuit events caused by overload, shoot-through, firmware errors, current surge and/or external fault conditions [1].

When a short-circuit event occurs, the system must detect the fault and safely turn-off the power devices to prevent catastrophic failure. To ensure fail-safe operations, power devices and gate drivers must work in synergy. The power devices must have a sufficiently long short-circuit withstanding time (SCWT) to survive high power dissipation before the protection circuitry is activated. The gate drivers must have a protection scheme with *(i)* fast response time to detect the short-circuit before devices fail, *(ii)* safe shutdown procedure to turn-off the devices without damage, and *(iii)* high noise immunity to prevent false trigger.

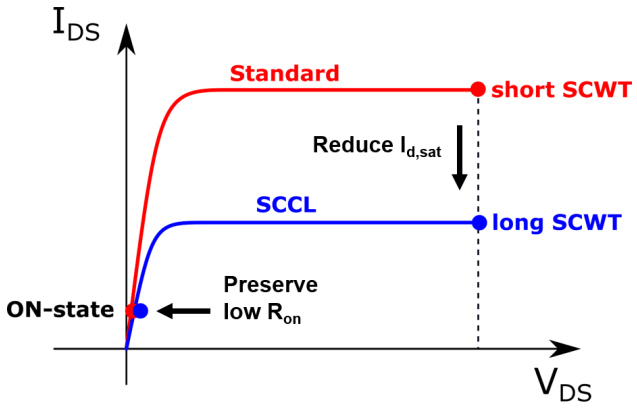

Fig. 1 The patented Short-Circuit Current Limiter (SCCL) reduces the drain-source saturation-current to increase the SCWT while preserving low on-state resistance.

Meeting these requirements at once can be challenging when using GaN. First, the inherently high power density of GaN HEMTs may pose limitations to their SCWT. When tested at 400 V, the SCWT of conventional 600-V GaN HEMTs available in the market has been limited to less than 0.5 µs [2] [3], too short for a reliable short-circuit protection. Second, the inherently fast switching of GaN HEMTs (dv/dt > 30 V/ns) poses stringent constraints on the noise immunity of the detection circuitry: short-circuit protection should not be erroneously activated during fast switching transients due to the natural drain current surge for capacitive charging and discharging.

In this work, we address these challenges and demonstrate successful synergy between GaN power devices and gate drivers to ensure short-circuit protection and survivability. We designed GaN power devices with Short-Circuit Current Limiter (SCCL) to achieve sufficiently long SCWT and paired them with a commercial gate driver with desaturation detection (DESAT) and soft shutdown circuitry, demonstrating an excellent protection response time of 800 ns, successful short-circuit

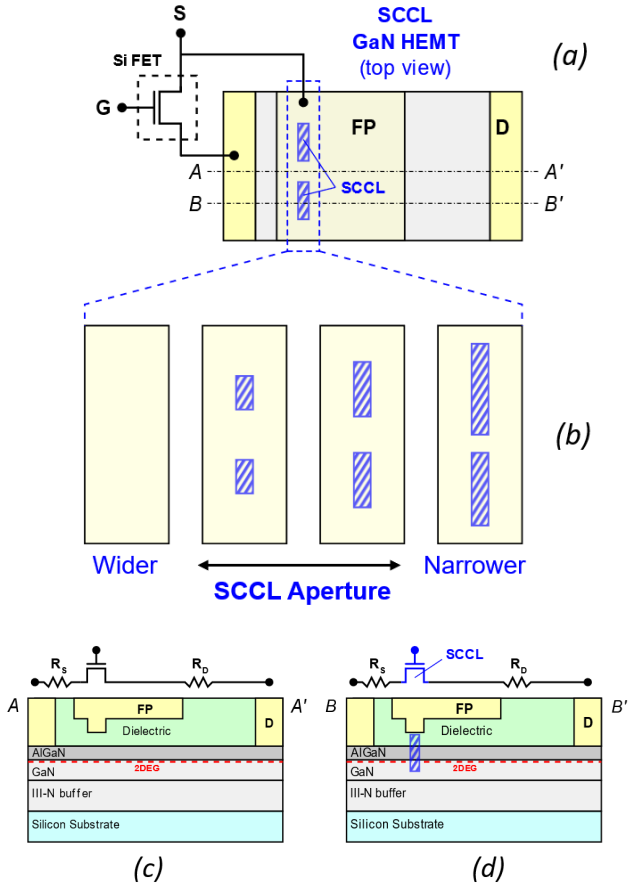

Fig. 2 *(a)* Top-view of two-chip normally-off GaN switch with the Short-Circuit Current Limiter (SCCL). The SCCL is implemented by removing segments of the 2DEG channel along the width of the GaN HEMT gate. *(b)* Top view of the HEMT gate with SCCL aperture series. The aperture can be easily tuned through a simple mask modification, to achieve a wide range of SCWT with limited Ron penalty. *(c)* and *(d)* Longitudinal cross-sections taken along path featuring the current aperture and the current block, respectively (Drawings are not to scale).

survival with high noise immunity up to the tested switching dv/dt of 100 V/ns.

II. GaN Power Devices with SCCL

During short-circuit events, GaN HEMTs are driven into saturation, simultaneously experiencing high voltage and high current, with consequent high power dissipation, rapid increase in temperature and catastrophic failures in a relatively very short time. A possible solution to increase the short-circuit withstanding time (SCWT) is to reduce the saturation current to reduce the dissipated power and slow down the temperature rise. In fact, the saturation current of standard GaN HEMTs is much in excess of the current usually required during normal operations—for example, 50-mΩ GaN devices operate at a current level no higher than 36 A in normal conditions [4], but during short-circuit events, the saturation current can be as high as 180 A. Therefore, we see an ample trade margin to reduce the saturation current to improve SCWT. The main challenge is doing so while preserving low on-state resistance, good

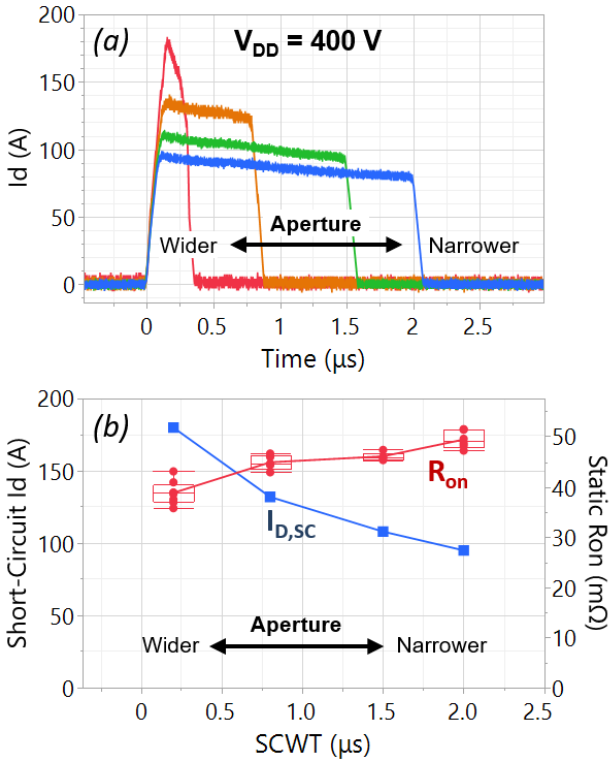

Fig. 3 (a) Short-circuit witshtanding time with a DC bus of 400 V and a fully-on gate-bias of 12 V on SCCL devices with multiple aperture sizes. *(b)* SCWT, short-circuit current and static Ron as a function of aperture size. Smaller aperture yields lower saturation current and longer SCWT, with only limited increase in Ron penalty.

switching performance and proven reliability (Fig. 1). In [5], we succeeded in such an endeavor with the patented Short-Circuit Current Limiter (SCCL), demonstrated using our 650-V normally-off two-chip core technology.

Transphorm's 650-V normally-off two-chip core technology consists of a low-voltage normally-off silicon FET connected in cascode configuration with a high-voltage normally-on GaN HEMT [6]. The Si-FET offers high threshold (+4 V), highest gate reliability and compatibility with standard gate drivers thanks to the robust SiO_2/Si MOS technology. The GaN HEMT is fabricated on silicon substrates for cost-effective manufacturing and has a field-plate to improve electric-field distribution and reliability. The gate of the GaN HEMT is isolated to suppress leakage current and off-state losses.

The Short-Circuit Current Limiter (SCCL) is implemented by removing segments of the 2DEG channel along the width of the HEMT gate (Fig. 2a), effectively creating a lateral current aperture. The aperture reduces the effective gate width of the device and its saturation current while preserving relatively low on-state resistance. Lower saturation current results in lower dissipated power during short-circuit events and longer withstanding time [7] [8]. The longitudinal cross-sections of the SCCL device are shown in Fig. 2c and Fig. 2d. The section *AA'* is taken along current aperture path, where the 2DEG is continuous from source to drain and electrons can flow in the

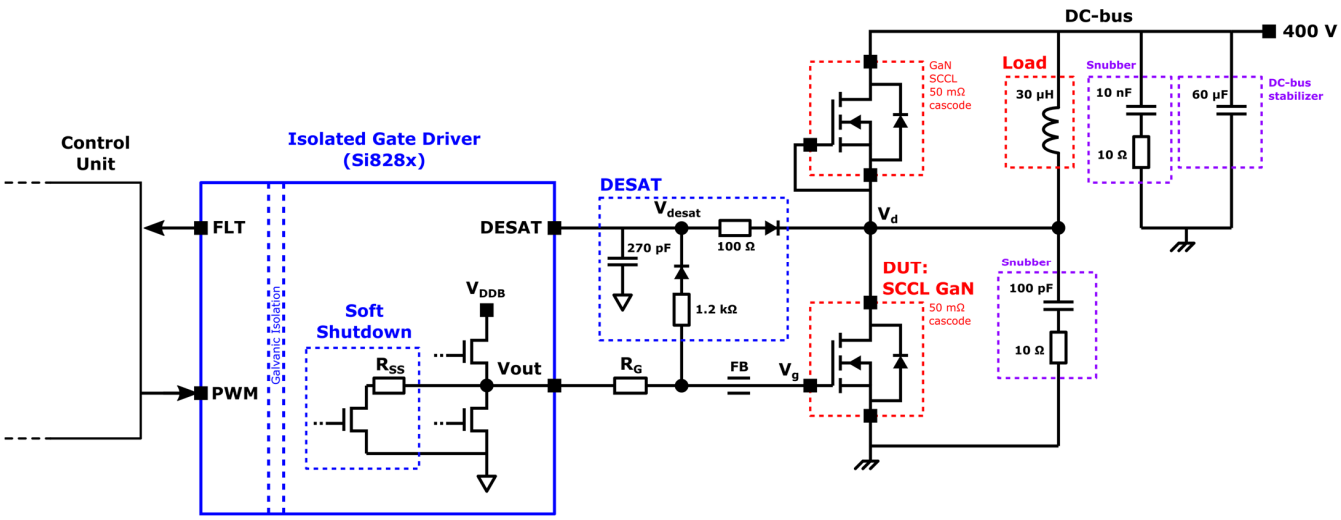

Fig. 4 Short-circuit protection circuitry using GaN power devices with Short-Circuit Current Limiter (SCCL) and a commercial insulated gate-driver with DESAT detection and soft shutdown. An RC network is inserted between the drain and the DESAT terminal to ensure good noise immunity.

on-state. In the aperture, the 2DEG density and mobility and the gate pinch-off voltage are the same as the standard device. The section *BB'* is taken along current-blocking path, showing the lack of 2DEG under the HEMT gate. The proper design of the current-blocking segmentation (length, width and periodicity of the current block areas) ensures a good control of the saturation current while maintaining a competitively low on-resistance. The SCCL is implemented under the HEMT gate for two reasons: *(i)* the gate is the most effective region to control the saturation current, and *(ii)* the access-region, which is a major component of the total on-state resistance, is not affected, therefore yielding relatively low R_{on} penalty.

The SCCL is implemented using a built-in proprietary process, does not require any additional process steps and does not add any additional process cost. The SCCL aperture can be easily formed and tuned through a simple mask plate modification. As demonstrated in [5], the SCCL does not introduce any additional charge trapping (same dynamic on-resistance), doesn't degrade the HEMT gate isolation (same off-state leakage) and has the same reliability than standard devices.

In [5], the SCCL aperture was tailored to achieve a SCWT of 3 µs at 400 V, resulting in an increase in on-state resistance of +0.35x with respect to standard devices without SCCL. In this work, we demonstrate the possibility to fine tune the SCWT and associated Ron penalty. We designed four different aperture sizes, from fully open (100%) to increasingly narrower (Fig. 2b). The short-circuit withstanding time of various apertures was then tested using a bus-voltage of 400 V and fully-on gate-bias of +12 V. Devices with the widest aperture (100% open, red curve in Fig. 3a) have an R_{on} of ~40 mΩ and show a short-circuit current of 180 A and a SCWT of only 0.3 µs. As we tested devices with narrower apertures, we measured lower short-circuit current and longer SCWT. The devices with the smallest aperture attempted in this work (blue curve in Fig. 3a) have a short-circuit current of 85 A resulting in a SCWT of 2 µs (7x higher than standard devices with full aperture) and a R_{on} penalty of only +0.27x. Please note, although the SCCL devices have lower saturation current than standard devices, $I_{d,sat}$ is still more than 2x higher than the rated DC-current needed during regular operations (36 A at room temperature for these devices), ensuring proper on-state operations and fast switching transients.

Thanks to its simplicity of implementation, the SCCL aperture and associated SCWT can be finely customized to match the timing requirements of any gate driver on the market, ensuring lowest R_{on} penalty.

III. Gate Drivers with DESAT Protection

To demonstrate how a GaN device with SCCL enables short-circuit protection with existing gate drivers, we carried out short-circuit protection experiments using a SCCL device coupled with a commercial gate driver with desaturation (DESAT) technology.

The short-circuit protection scheme is depicted in Fig. 4. The power stage has two identical GaN power devices in half-bridge configuration: the low-side device is the active DUT being tested under short-circuit and switching conditions; the high-side device is used as free-wheeling diode to recycle the inductor current. The power devices are assembled in a well-known, high thermal conduction TO-247 package. We selected devices with a current limiter tuned for a SCWT of 1.5 µs and an R_{on} penalty of only +0.2x. Relatively short SCWT and small R_{on} penalty are possible thanks to the adoption of a gate driver with fast fault detection circuitry.

The gate driver is a commercially available Skyworks Si828x with galvanic isolation to ensure fail-safe operations and avoid any damage to the control electronics. The short-circuit protection is implemented through desaturation detection (DESAT). When the gate is on, the DESAT circuitry monitors the drain voltage of the power device: if the drain voltage becomes higher than a certain threshold (nominally 7 V), the

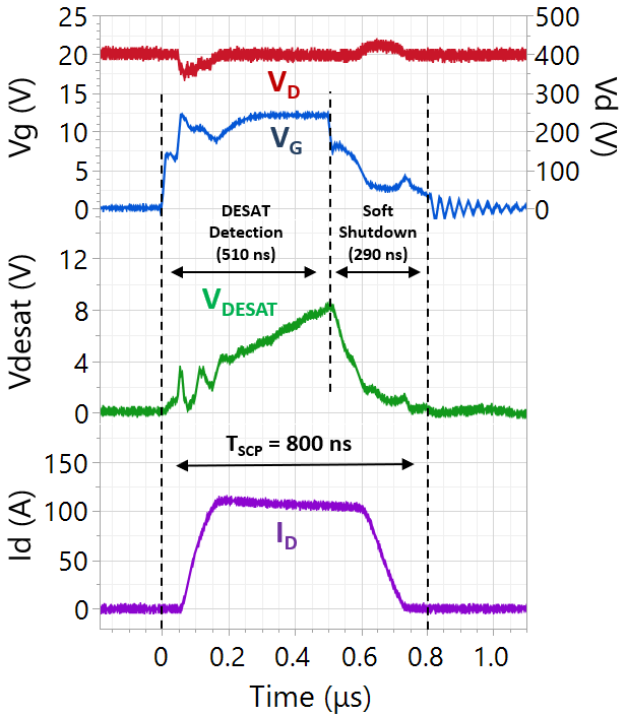

Fig. 5 Short-circuit protection of a SCCL device paired with a gate driver with DESAT detection. Thanks to DESAT and soft shutdown, the short-circuit is detected and shutdown in 800 ns, a period sufficiently short to ensure the survival of the SCCL power device with ample margin. In fact, the device current limiter has been tuned for a SCWT of 1.5 µs. The GaN power device with SCCL technology succesfully survived the short-circuit event for all 100 repetitions.

TABLE I. DEVICE PARAMETERS, PRE-POST SC TEST

Parameter	Pre SC Test	Post SC Test	Conditions
Static Ron (mΩ)	47	46	I_d = 8 A
Dynamic Ron (mΩ)	55	54	I_d = 8 A
Threshold Voltage (V)	4.1	4.1	I_d = 1 mA
Gate Leakage (nA)	0.4	0.5	(V_g;V_d) = (20V;0V)
Drain Leakage (µA)	2.2	1.8	(V_g;V_d) = (0V;750V)

gate driver raises a flag (FLT) and triggers the soft shutdown of the power device. To ensure noise immunity, an RC network is inserted between the drain and the DESAT terminal. This network introduces a delay in the rise of the DESAT voltage (V_{DESAT}). If no delay is introduced, the DESAT could be erroneously triggered by system noise or by the natural surge in drain current due to capacitive charging & discharging during switching transients.

Once a short-circuit event is detected with the DESAT circuitry, the power device is safely turned-off using a soft shutdown procedure. The soft shutdown is implemented through an alternative gate loop with a higher resistance (R_{SS} = 68 Ω)

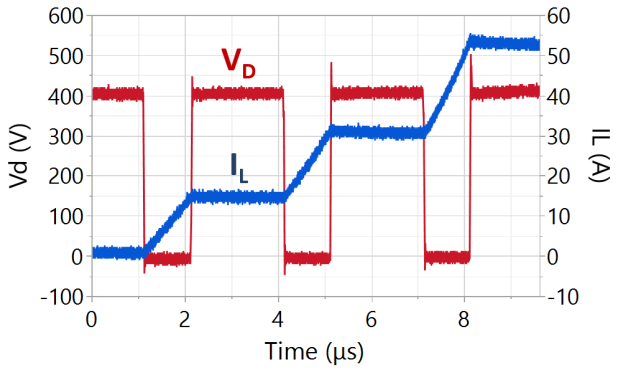

Fig. 6 Succesful inductive switching of a SCCL GaN device with a gate driver with DESAT circuitry. With an R_g of 30 Ω, we measured a dv/dt of ~35 V/ns in both turn-on and turn-off transients. With an R_g of 10 Ω, we recorded a maximum dv/dt of more than 100 V/ns during turn-off. The short-circuit protection has never been triggered during switching transients, indicating good noise immunity.

[9]. Higher gate resistance during short-circuit shutdown is required to slow down the turn-off transient and to avoid excessive drain voltage surge due to high di/dt (during short-circuit events, the drain current is much higher than in regular operations, therefore requiring softer turn-off).

To verify the functionality and good noise immunity of our short-circuit protection, we carried out both short-circuit protection tests and inductive switching tests. The load inductor is set to 30 µH. A 60-µF capacitance is added to the DC-bus to stabilize the supply voltage. RC snubbers of (10 nF + 10 Ω) and (100 pF + 10 Ω) are connected to the DC-bus and switching node, respectively. A gate resistor (R_G) of 30 Ω and a ferrite bead of 220 Ω at 100 MHz are added to the gate loop. In this work, all tests have been carried out at room-temperature with a DC-bus of 400 V.

A. Short-Circuit Protection Results

During short-circuit protection tests, the load inductance is short-circuited and the gate is fully turned (+12 V) on directly into a fault, a worst-case scenario referred to as "hard-switch fault."

The short-circuit waveforms are shown in Fig. 5. As the gate is fully turned-on into the fault, the drain current reaches 110 A (the saturation level set by the SCCL aperture). At the same time, V_{DESAT} rises and reaches the fault threshold in 510 ns. At this point, the fault flag is raised, and the soft shutdown procedure is initiated. The gate voltage slowly decreases reaching 0 V in 290 ns. Thanks to the soft shutdown, the drain voltage surges to only 430 V—well within the maximum rated voltage (650 V), with no risks of device degradation nor catastrophic breakdown. The overall Short-Circuit Protection Response Time (T_{SCP}) is the time elapsed between the device turn-on into the fault and the complete device shutdown, comprising of both DESAT detection time and soft-shutdown time. With our protection scheme, T_{SCP} is 800 ns, sufficiently short to ensure the survival of the SCCL power device with ample margin. The T_{SCP} is almost 2x shorter than the device SCWT. This would have not been possible with standard

devices, where the SCWT is too short, causing device failure before the protection response would be completed.

To ensure the robustness of our protection scheme, we carried out repetitive tests, delivering 100 short-circuit pulses at intervals of 30 seconds. The power device survived all the 100 short-circuit events at 400 V without failure and with no significant degradation of the main device parameters, including static R_{on}, dynamic R_{on}, threshold voltage, gate leakage and off-state drain leakage (Table I). This indicates no significant damage has been created in the power device during short-circuit events and associated protection process.

B. Inductive Switching Test Results

To verify the switching performance of SCCL devices and the noise immunity of our short-circuit protection, we carried out inductive switching tests. The DC-bus voltage is set to 400 V and the load inductor current is ramped from 0 A to ~50 A through multiple 1-µs pulses (Fig. 6). With an R_G of 30 Ω, we measured a dv/dt of ~35 V/ns in both turn-on and turn-off transients. Successfully, the DESAT potential never reached the fault threshold. No false short-circuit fault was flagged and no undesired shutdown procedure was initiated.

To test the noise immunity of the DESAT circuitry to an even higher switching speed, we decreased the R_G to 10 Ω recording a maximum turn-off dv/dt of more than 100 V/ns during turn-off transient. Even in this case, the short-circuit protection was not erroneously activated, indicating good noise immunity and excellent versatility to diverse switching conditions.

IV. Conclusions

In this work, we have demonstrated a successful short-circuit protection for a GaN power device equipped with Short-Circuit Current Limiter (SCCL) and a commercial gate driver with DESAT detection and soft shutdown circuitry. The short-circuit withstanding time of GaN devices can be easily tuned by adjusting the SCCL aperture size. In this work, the SCWT was tuned in the range from 0.3 µs to 2 µs at 400 V, demonstrating a remarkable 7x increase with a relatively small penalty in on-state resistance. The gate-driver has DESAT, soft shutdown circuitry and high noise immunity. This protection scheme has a response time of 800 ns ensuring the survival of GaN devices with SCCL, and offers high switching performance and high noise immunity to values greater than 100 V/ns. The combination of a GaN power device with SCCL and a commercial gate driver with fast DESAT and high noise immunity allows short-circuit protection and fail-safe operation of GaN power electronics for additional robustness in motor drive applications.

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