Short-Circuit Capability with GaN HEMTs

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***Abstract*—Short-circuit capability with GaN HEMTs is demonstrated thanks to an integrated Short-Circuit Current Limiter (SCCL) and a commercial gate-driver with DESAT protection. The SCCL is applied to GaN HEMTs to achieve a sufficiently long short-circuit withstanding time (SCWT) while retaining competitive on-state resistance. The SCWT is tuned from 0.3 µs to 3 µs (a remarkable 10x increase) with a relatively small penalty in on-resistance, no leakage increase, no threshold voltage degradation and no reliability degradation. The gate-driver has desaturation detection (DESAT) and soft shutdown circuitry to achieve a fast protection response of 800 ns with high noise immunity greater than 100 V/ns. The combination of GaN power devices with SCCL and a commercial gate driver with fast DESAT and high noise immunity allows short-circuit protection and fail-safe operation of GaN power electronics for additional robustness in motor drive applications.**

***Index Terms*—Current Limiter, DESAT, GaN, HEMT, Short-Circuit**

I. Introduction

High-efficiency GaN power devices are penetrating several power electronics markets, including adapters, power supply units, photovoltaic inverters, battery chargers, and motor drives.

When used in motor drive applications, GaN power devices must not only pass stringent JEDEC or AEC-Q0101 reliability tests, but also be short-circuit capable. GaN devices may be required to survive short-circuit events caused by overload, shoot-through, firmware errors, current surge and/or external fault conditions (Fig. 1) [1].

When a short-circuit event occurs, the system must detect the fault and safely turn-off the power devices to prevent catastrophic failure. The fault detection can be added to the gate-driver with protection circuitry such as desaturation detection (DESAT) or over-current sensing (OC) [2]. To ensure fail-safe operations, power devices and gate drivers must work in synergy. The response time of the protection circuitry must be carefully tuned: if the response time is too fast, the protection circuitry may have poor noise immunity and be erroneously activated by glitches, noise, and switching transients. If the response time is too slow, the power device may fail before the protection system is activated, posing a dangerous hazard for systems and users.

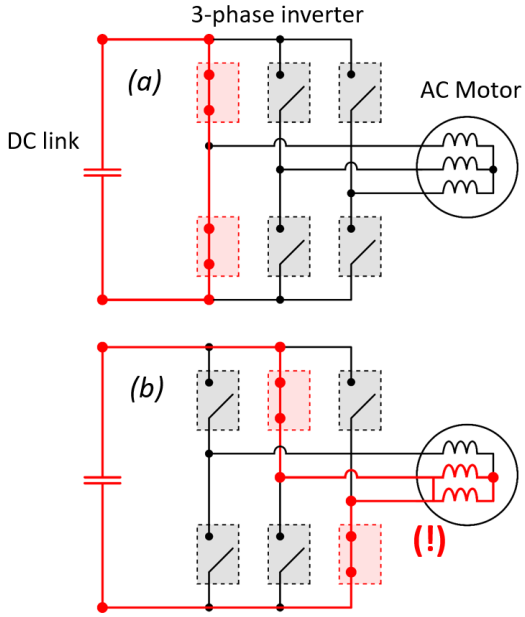

Fig. 1 Power devices in a 3-phase motor drive, showing two short-circuit scenarios: *(a)* shoot-through between high-side and low-side and *(b)* short-circuit across the inductive load.

With commercial gate drivers, an adequate response period is in the range of 1 µs [3]. During this period, the power device must withstand the short-circuit condition without failing. Hence the need to define an important device requirement: the Short-Circuit Withstanding Time (SCWT), i.e., the minimum period a device is capable to withstand a short-circuit event, with both high voltage and high current applied between source and drain terminals.

One of the main factors affecting the SCWT of any given device technology is the thermally-induced catastrophic failure [4] [5]. During short-circuit conditions, the device is subjected to both high voltage and high current; a condition that leads to

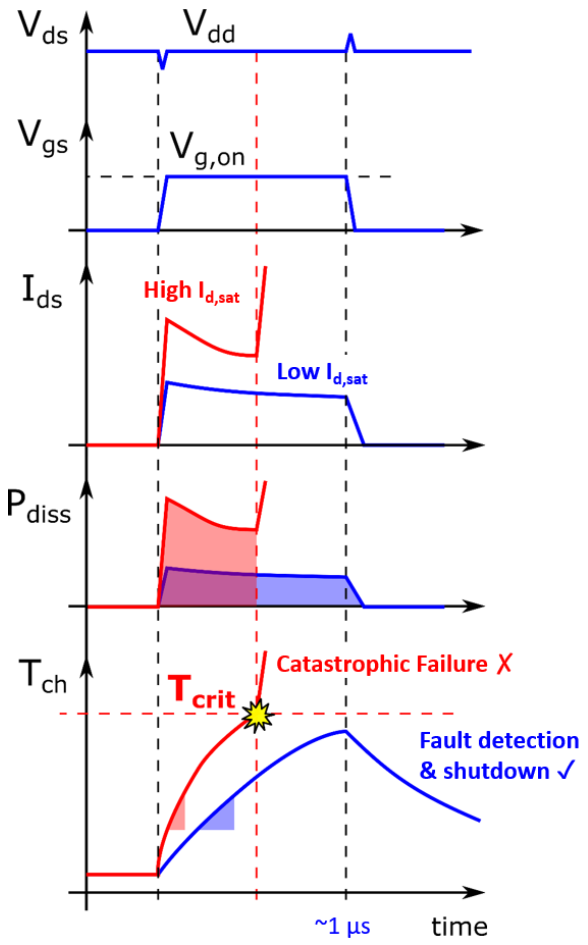

Fig. 2 Schematic waveforms during short-circuit condition for *(a)* a device with high current and power density leading to steep temperature rise and catastrophic failure before the protection circuitry could intervene and *(b)* a device with lower current and lower power density, allowing the protection circuitry to detect the fault and safely turn-off the device before the critical temperature to failure is reached.

enormous instantaneous power dissipation and rapid increase in temperature until one or more failure mechanisms are triggered and the catastrophic failure happens (Fig. 4, red curve). To improve SCWT, it is therefore important to limit the power dissipated during a short-circuit event, so that the protection circuitry can intervene before the critical temperature to failure is reached (Fig. 4, blue curve). The biggest challenge is doing so while maintaining high device performance (low on-state resistance, low capacitance and fast switching) and long-term reliability.

In conventional silicon-based power-devices, such as Si IGBTs, the SCWT can be greater than 10 µs [6]. On the other hand, ensuring a high SCWT in wide-band gap (WBG) devices such as SiC MOSFETs or GaN HEMTs is more challenging. Due to their own nature and virtue, WBG devices can deliver much higher power density in smaller areas than conventional silicon devices. Consequently, they may experience a steeper rise in temperature during short-circuit events resulting in shorter SCWT than silicon-based counterparts.

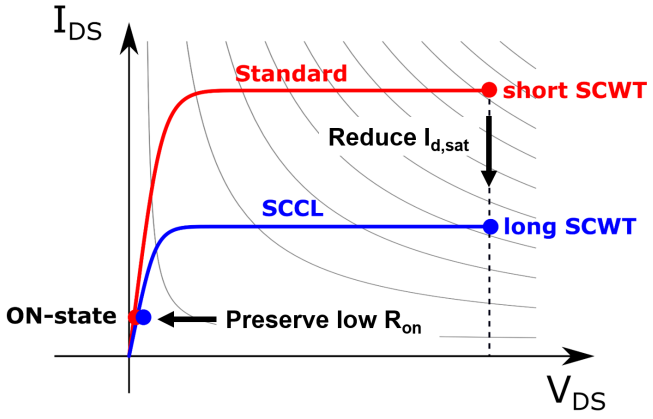

Fig. 3 The patented Short-Circuit Current Limiter (SCCL) reduces the drain-source saturation-current to increase the SCWT while preserving low on-state resistance. Dissipated power contour lines are shown in the background. During short-circuit events, lower saturation-current yields lower dissipated power and longer witshtading time.

SiC devices show a strong trade-off between SCWT and performance: SiC devices optimized for low specific on-resistance ($R_{on,sp}$) suffer from short SCWT. In Ref. [7], SiC MOSFETs with increasingly short gate length show not only the desired three-fold reduction in $R_{on,sp}$ from 21.5 mΩ·cm^2 to 7.5 mΩ·cm^2, but also a remarkable, undesired three-fold reduction in SCWT from 9 µs to 2.7 µs. Data in [8] shows a similar trend. When the density of MOS-cells is increased, the $R_{on,sp}$ is improved, but the SCWT is strongly reduced. Smaller $R_{on,sp}$ leads to higher power-density, but comes with a cost of smaller SCWT due to faster thermal failure.

Up until now, a similar scenario has been observed with GaN devices. An early research work by Nagahisa *et al.* [5] shows a 600-V GaN technology with a SCWT ≥ 3 µs at 400 V. However, according to the data reported in the paper, the normalized R_{on} of that technology is greater than 20 Ω·mm (> 9 mΩ·cm^2), relatively high to be adopted by the market. On the other hand, when 600-V GaN devices have been designed with a competitive $R_{on,sp}$ to be commercially competitive, they have shown a SCWT limited to less than 0.5 µs at 400 V [9] [10] [11], too short for a reliable short-circuit protection.

Although the failure mechanisms are still object of research [12] [13] [14] [15] [16], one of the causes limiting the SCWT of commercial GaN HEMTs could be ascribed to high current density. The 2DEG forming at the AlGaN/GaN interface has a charge density of ~1x10^{13} electrons/cm^2 and a mobility as high as 2000 cm^2/V·s, resulting in high current density up to 1 A/mm, which causes high power-density and a steep temperature rise during short-circuit events.

If the industry relies on conventional GaN HEMTs, non-ideal constrains would be needed for ultra-fast short-circuit protection circuitry [11] [17] [18]. This scenario comes with very limited room for blanking-time and higher risks of false trigger in noisy industrial and automotive environments.

Alternatively, and preferably, engineering solutions can be implemented at a device-level to increase SCWT while

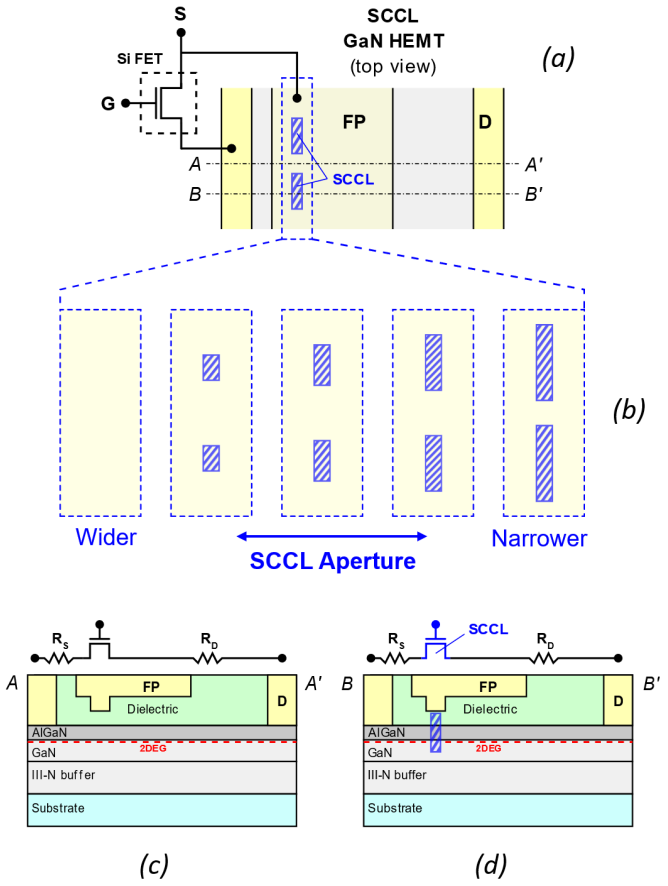

Fig. 4 *(a)* Top-view of two-chip normally-off GaN switch with the Short-Circuit Current Limiter (SCCL). The SCCL is implemented by removing segments of the 2DEG channel along the width of the GaN HEMT gate. *(b)* Top view of the HEMT gate with SCCL aperture series. The aperture can be easily tuned through a simple mask modification, to achieve a wide range of SCWT with limited Ron penalty. *(c)* and *(d)* Longitudinal cross-sections taken along path featuring the current aperture and the current block, respectively (Drawings are not to scale).

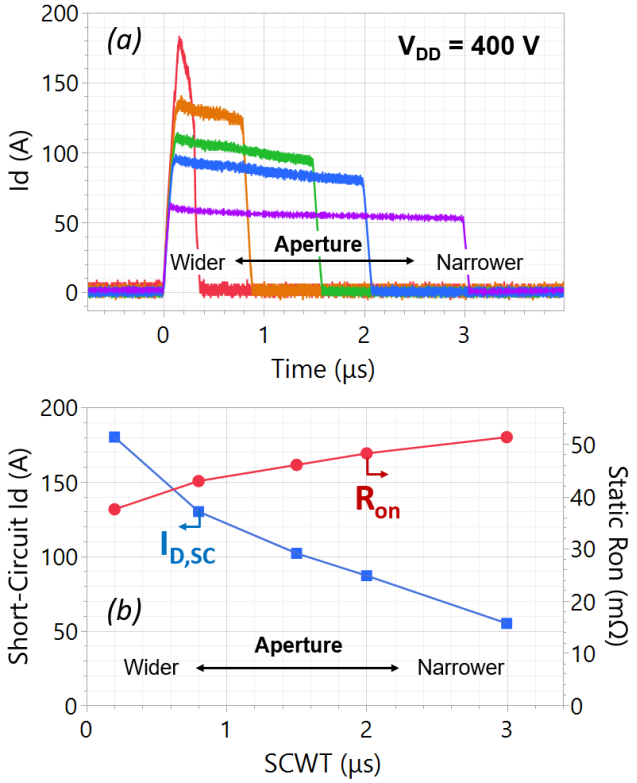

Fig. 5 (a) Short-circuit witshtanding time with a DC bus of 400 V and a fully-on gate-bias of 12 V on SCCL devices with multiple aperture sizes. *(b)* SCWT, short-circuit current and static Ron as a function of aperture size. Smaller aperture yields lower saturation current and longer SCWT, with only limited increase in Ron penalty.

preserving high performance (low specific on-resistance and low switching time) and high reliability.

In this work, we address these challenges and demonstrate successful synergy between GaN power devices and gate drivers to ensure short-circuit capability with sufficient noise immunity. First, we demonstrate GaN power devices with Short-Circuit Current Limiter (SCCL) to achieve sufficiently long SCWT while retaining competitive on-state resistance and highest reliability. Second, we pair SCCL devices with a commercial gate driver with desaturation detection (DESAT) and soft shutdown circuitry, and we demonstrate successful short-circuit survival with a protection response time of 800 ns and high noise immunity up to the tested switching dv/dt of 100 V/ns.

II. GaN HEMTs with SCCL

During short-circuit events, GaN HEMTs are driven into saturation, simultaneously experiencing high voltage and high current, with consequent high power dissipation, rapid increase in temperature and catastrophic failures in a relatively very short time. A possible solution to increase the short-circuit withstanding time (SCWT) is to reduce the saturation current to reduce the dissipated power and slow down the temperature rise.

This solution has been patented for GaN devices [19] [20], and referred to as Short-Circuit Current Limiter (SCCL) (Fig. 3) [21]. In a two-chip normally-off solution, lower short-circuit current and higher SCWT can be achieved by controlling either the saturation-current of the Si-FET or the saturation-current of the GaN-HEMT. In this work, we demonstrate the latter: increasing SCWT by reducing the $I_{d,sat}$ of the GaN-HEMT.

The SCCL is demonstrated using Transphorm's 650-V normally-off two-chip core technology, consisting of a low-voltage normally-off silicon FET connected in cascode configuration with a high-voltage normally-on GaN HEMT [22]. The Si-FET offers high threshold (>3.5 V), highest gate reliability and compatibility with standard gate drivers thanks to the robust SiO_2/Si MOS technology. The GaN HEMT is fabricated on silicon substrates for cost-effective manufacturing and has a field-plate to improve electric-field distribution and reliability. The gate of the GaN HEMT is isolated to suppress leakage current and off-state losses.

The Short-Circuit Current Limiter (SCCL) is implemented by removing segments of the 2DEG channel along the width of the HEMT gate (Fig. 4a), effectively creating a lateral current

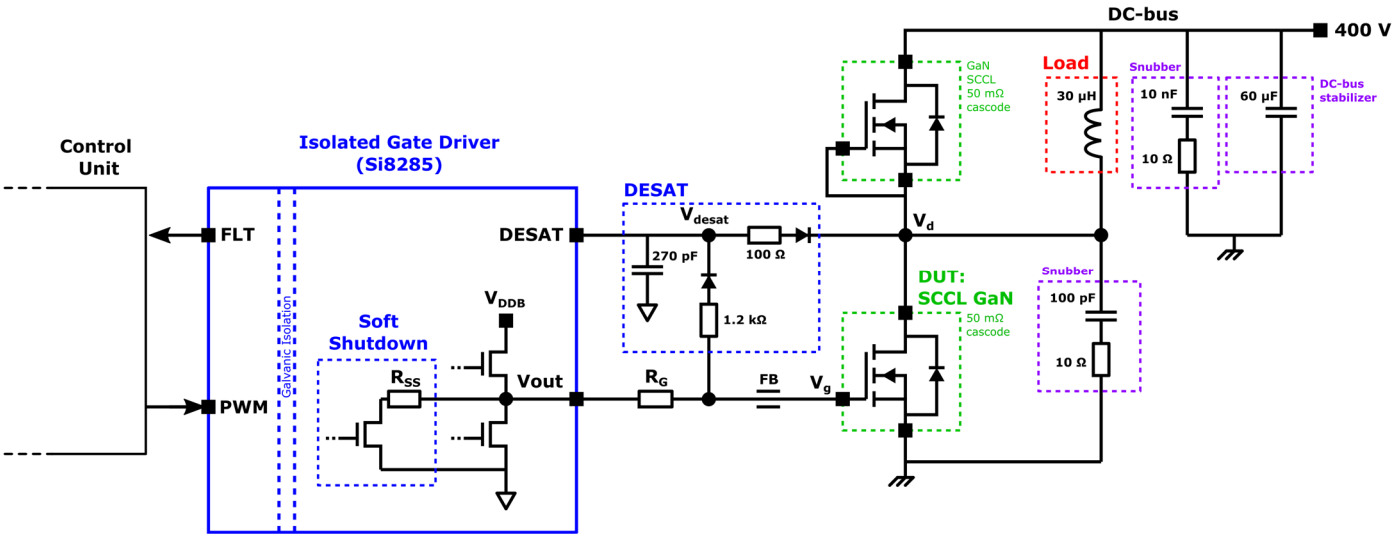

Fig. 6 Short-circuit protection circuitry using GaN power devices with Short-Circuit Current Limiter (SCCL) and a commercial gate-driver with DESAT detection and soft shutdown. An RC network is inserted between the drain and the DESAT terminal to ensure good noise immunity.

aperture. The aperture reduces the effective gate width of the device and reduces its saturation current while preserving relatively low on-state resistance. During short-circuit events, lower saturation current results in lower dissipated power and longer withstanding time. The longitudinal cross-sections of the SCCL device are shown in Fig. 4c and Fig. 4d. The section *AA'* is taken along current aperture path, where the 2DEG is continuous from source to drain and electrons can flow in the on-state. In the aperture, the 2DEG charge density and mobility are the same as in the standard device. The section *BB'* is taken along current-blocking path, showing the lack of 2DEG under the HEMT gate. The proper design of the current-blocking segmentation (length, width and periodicity of the current block areas) ensures a good control of the saturation current while maintaining a competitively low on-resistance. The SCCL is implemented under the HEMT gate for two reasons: *(i)* the gate is the most effective region to control the saturation current, and (*ii)* the access-region, a major component of the total on-state resistance, is not affected, therefore yielding relatively low R_{on} penalty.

The SCCL is implemented using a built-in proprietary process, does not require any additional process steps and does not add any additional process cost. The SCCL aperture can be easily formed and tuned through a simple mask plate modification. The SCCL does not introduce any additional charge trapping (same dynamic on-resistance), doesn't degrade the HEMT isolation (same off-state leakage), doesn't affect the Si-FET gate properties (same threshold and gate leakage) and has the same reliability than standard devices.

The SCCL aperture can be precisely tuned to obtain the desired SCWT with minimal Ron penalty. To demonstrate the SCCL tunability, we designed five different aperture sizes, from fully open (100%) to increasingly narrower (Fig. 4b). The short-circuit withstanding time of various apertures was then tested using a bus-voltage of 400 V and fully-on gate-bias of +12 V. Devices with the widest aperture (100% open, red curve in Fig. 5a) have an R_{on} of ~40 mΩ and show a short-circuit current of 180 A and a SCWT of only 0.3 µs. Devices with incrementally narrower apertures have incrementally lower short-circuit current and longer SCWT. The devices with the smallest aperture attempted in this work (blue curve in Fig. 5a) have a short-circuit current of only 55 A resulting in a SCWT of 3 µs (10x higher than standard devices with full aperture) and a R_{on} penalty of +0.35x.

Thanks to its simplicity of implementation, the SCCL aperture and associated SCWT can be finely customized to match the timing requirements of any gate driver on the market, ensuring lowest R_{on} penalty.

III. Gate Drivers with DESAT Protection

To demonstrate how a GaN device with SCCL enables short-circuit protection with existing gate drivers, we carried out short-circuit protection experiments using a SCCL device coupled with a commercial gate driver with desaturation technology (DESAT).

The short-circuit protection scheme is depicted in Fig. 6. The power stage has two identical GaN power devices with SCCL in half-bridge configuration: the low-side device is the active DUT being tested under short-circuit and switching conditions; the high-side device is used as free-wheeling diode to recycle the inductor current. The power devices are assembled in a well-known, high-thermal-conductivity TO-247 packages. We selected SCCL devices with a current limiter tuned for a SCWT of 1.5 µs, a saturation current of less than 110 A, and a R_{on} penalty of only +0.2x. Please note, although the SCCL devices have lower saturation current than standard devices, $I_{d,sat}$ is still ~3x higher than the rated DC-current needed during regular operations (36 A at room temperature for these devices), ensuring proper on-state operations and fast switching transients.

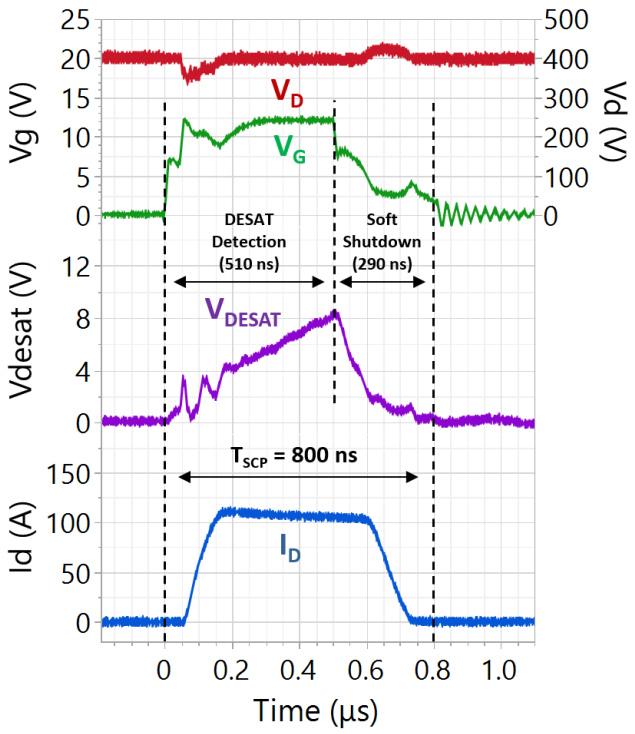

Fig. 7 Short-circuit protection of a SCCL device tuned for a SCWT of 1.5 µs paired with a gate driver with DESAT detection. Thanks to DESAT and soft shutdown, the short-circuit is detected and shutdown in 800 ns, a period sufficiently short to ensure the survival of the SCCL power device with ample margin. The GaN power device with SCCL technology succesfully survived the short-circuit event for all 100 repetitions.

TABLE I. DEVICE PARAMETERS, PRE-POST SC TEST

Parameter	Pre SC Test	Post SC Test	Conditions
Static Ron (mΩ)	47	46	I_d = 8 A
Dynamic Ron (mΩ)	55	54	I_d = 8 A
Threshold Voltage (V)	4.1	4.1	I_d = 1 mA
Gate Leakage (nA)	0.4	0.5	(V_g;V_d) = (20V;0V)
Drain Leakage (µA)	2.2	1.8	(V_g;V_d) = (0V;750V)

The gate driver is a commercially available Skyworks Si8285 with galvanic isolation to ensure fail-safe operations and avoid any damage to the control electronics. The short-circuit protection is implemented through desaturation detection (DESAT). When the gate is on, the DESAT circuitry monitors the drain voltage of the power device: if the drain voltage becomes higher than a certain threshold (nominally 7 V), the gate driver raises a flag (FLT) and triggers the soft shutdown of the power device. To ensure noise immunity, an RC network is inserted between the drain and the DESAT terminal. This network introduces a delay in the rise of the DESAT voltage (V_{DESAT}). If no delay is introduced, the DESAT could be

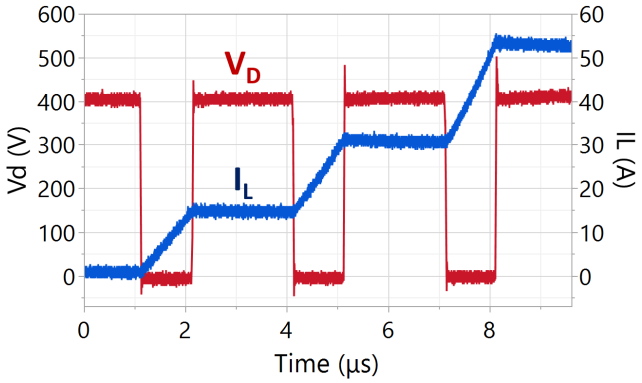

Fig. 8 Succesful inductive switching of a SCCL GaN device with a gate driver with DESAT circuitry. With an R_g of 30 Ω, we measured a dv/dt of ~35 V/ns in both turn-on and turn-off transients. With an R_g of 10 Ω, we recorded a maximum dv/dt of more than 100 V/ns during turn-off. The short-circuit protection is triggered during switching transients, indicating good noise immunity.

erroneously triggered by system noise or by the natural surge in drain current due to capacitive charging & discharging during switching transients.

Once a short-circuit event is detected with the DESAT circuitry, the power device is safely turned-off using a soft shutdown procedure. The soft shutdown is implemented through an alternative gate loop with a higher resistance (R_{SS} = 68 Ω) [9]. Higher gate resistance during short-circuit shutdown is required to slow down the turn-off transient and avoid excessive drain voltage surge due to high di/dt (during short-circuit events, the drain current is higher than in regular operations, therefore requiring softer turn-off).

To verify the functionality and good noise immunity of our short-circuit protection, we carried out both short-circuit protection tests and inductive switching tests. The load inductor is set to 30 µH. A 60-µF capacitance is added to the DC-bus to stabilize the supply voltage. RC snubbers of (10 nF + 10 Ω) and (100 pF + 10 Ω) are connected to the DC-bus and switching node, respectively. A gate resistor (R_G) of 30 Ω and a ferrite bead of 220 Ω at 100 MHz are added to the gate loop. In this work, all tests have been carried out at room-temperature with a DC-bus of 400 V.

A. Short-Circuit Protection Results

During short-circuit protection tests, the load inductance is short-circuited and the gate is fully turned on (+12 V) directly into a fault, a worst-case scenario referred to as "hard-switch fault."

The short-circuit waveforms are shown in Fig. 7. As the gate is fully turned-on into the fault, the drain current reaches 108 A (the saturation level set by the SCCL aperture). At the same time, V_{DESAT} rises and reaches the fault threshold in 510 ns. At this point, the fault is flagged, and the soft shutdown procedure is initiated. The gate voltage decreases reaching 0 V in 290 ns. Thanks to the soft shutdown, the drain voltage surges to only 430 V—well within the maximum rated voltage (650 V), with no risks of device degradation nor catastrophic breakdown. The overall Short-Circuit Protection Response Time (T_{SCP}) is the

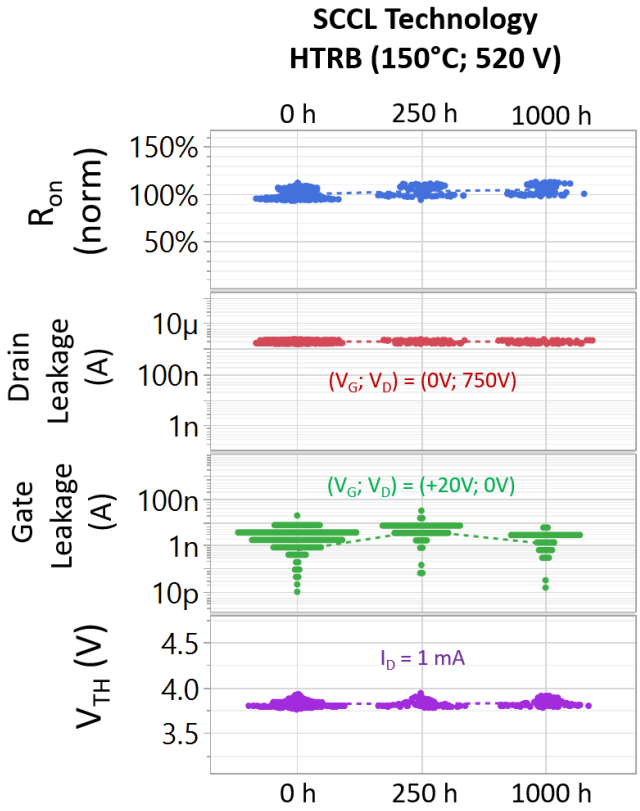

Fig. 9 On-state resistance, drain leakage, gate leakage and threshold voltage measured before and after 1000-h HTRB carried out at 150°C and 520 V on SCCL GaN devices (80 parts). After both 250 and 1000 hours, we observed no fuse failure, no leakage increase, no threshold voltage shift and a relatively small parametric Ron degradation (~5%). The small parametric Ron degradation is similar to what observed in standard devices, therefore indicating that the SCCL blocking region does not introduce any additional degradation and/or failure mechanisms.

time elapsed between the device turn-on into the fault and the complete device shutdown, comprising of both DESAT detection time and soft-shutdown time. With our protection scheme, T_{SCP} is 800 ns, sufficiently short to ensure the survival of the SCCL power device with ample margin. The T_{SCP} (800 ns) is almost 2x shorter than the device SCWT (1.5 µs). This would have not been possible with standard devices with a too short SCWT.

To ensure the robustness of our protection scheme, we carried out repetitive tests, delivering 100 short-circuit pulses at intervals of 30 seconds. The power device survived all the 100 short-circuit events at 400 V without failure and with no significant degradation of the main device parameters, including static R_{on}, dynamic R_{on}, threshold voltage, gate leakage and off-state drain leakage (Table I). This indicates no significant damage has been created in the power device during short-circuit events and associated protection process.

B. Inductive Switching Test Results

To verify the switching performance of SCCL devices and the noise immunity of our short-circuit protection, we carried out inductive switching tests. The DC-bus voltage is set to 400 V and the load inductor current is ramped from 0 A to ~50 A through multiple 1-µs pulses (Fig. 8). With an R_G of 30 Ω, we measured a dv/dt of ~35 V/ns in both turn-on and turn-off transients, similar switching performance than standard GaN power devices tested in the same conditions. Successfully, the DESAT potential never reached the fault threshold. No false short-circuit fault was flagged and no undesired shutdown procedure was initiated.

To test the noise immunity of the DESAT circuitry to an even higher switching speed, we decreased the R_G to 10 Ω recording a maximum turn-off dv/dt of more than 100 V/ns during turn-off transient. Even in this case, the short-circuit protection was not erroneously activated, indicating good noise immunity and excellent versatility to diverse switching conditions.

IV. RELIABILITY

To further assess the reliability of SCCL devices, we submitted 80 parts to a High-Temperature Reverse-Bias (HTRB) at 150°C and 520 V for 1000 hours. Full parametric characterization has been carried out at the beginning (t = 0 h), interim (t = 250 h), and at the end of the stress campaign (t = 1000 h). Results are reported in Fig. 9. After both 250 hours and 1000 hours, we observed no fuse failure, no leakage increase, no threshold voltage shift and a relatively small parametric R_{on} degradation (~5%). The small parametric R_{on} degradation is similar to what observed in standard devices, therefore indicating that the SCCL blocking region does not introduce any additional degradation and/or failure mechanisms. This is a promising result towards the prospective JEDEC and automotive qualifications of SCCL technology.

V. CONCLUSIONS

In this work, we have demonstrated short-circuit capability with GaN HEMTs. Our solution comprises of GaN power devices equipped with Short-Circuit Current Limiter (SCCL) paired with a commercial gate driver with DESAT detection and soft shutdown circuitry. The short-circuit withstanding time of GaN devices can be easily tuned by adjusting the SCCL aperture size, while retaining competitive on-state resistance, low leakage and highest reliability. In this work, the SCWT was tuned in the range from 0.3 µs to 3 µs at 400 V, demonstrating a remarkable 10x increase with a relatively small penalty in on-state resistance. The gate-driver has DESAT, soft shutdown circuitry and high noise immunity. The protection scheme has a response time of 800 ns ensuring the survival of GaN devices with SCCL, and offers high switching performance and high noise immunity to values greater than 100 V/ns. The SCCL technology has demonstrated to have the similar switching performance and reliability than the standard Transphorm technology. The combination of a GaN power device with SCCL and a commercial gate driver with fast DESAT and high noise immunity allows short-circuit protection and fail-safe operation of GaN power electronics for additional robustness in motor drive applications.

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